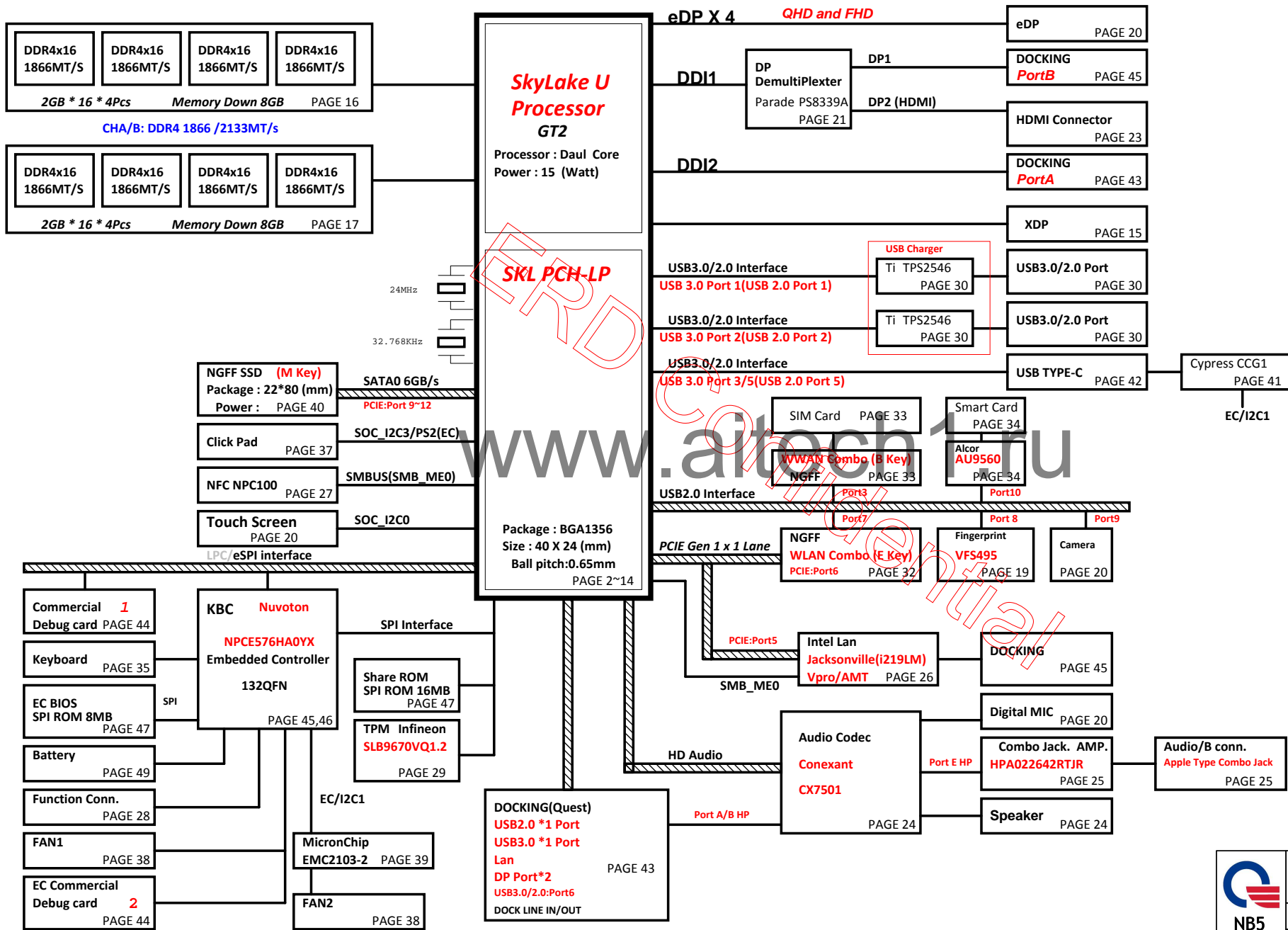


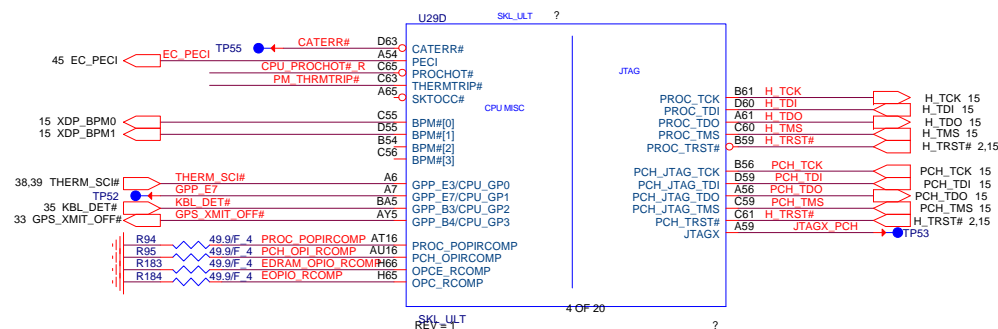
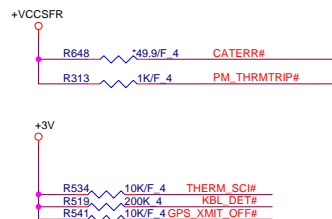
# 2015 Bellagio 1.0,14"UMA Schematics

PCB 10L STACK UP(1.0mm)

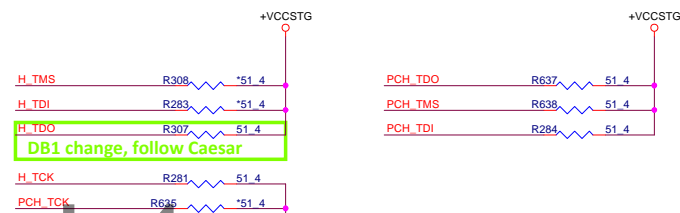
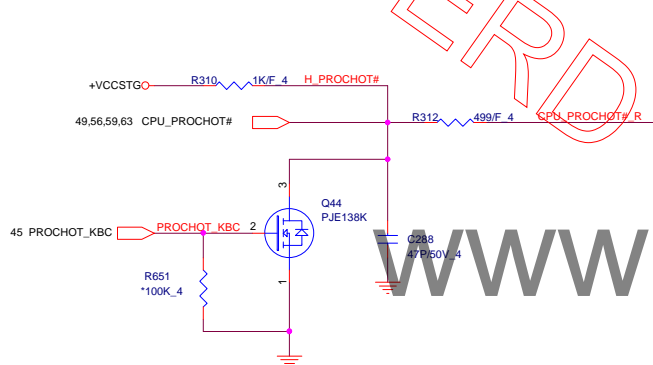
01

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(High)  
LAYER 5 : SGND  
LAYER 6 : SVCC  
LAYER 7 : IN3(High/Low)  
LAYER 8 : IN4(HIGH)  
LAYER 9 : SGND  
LAYER 10 : BOT





### Processor pull-up (CPU)

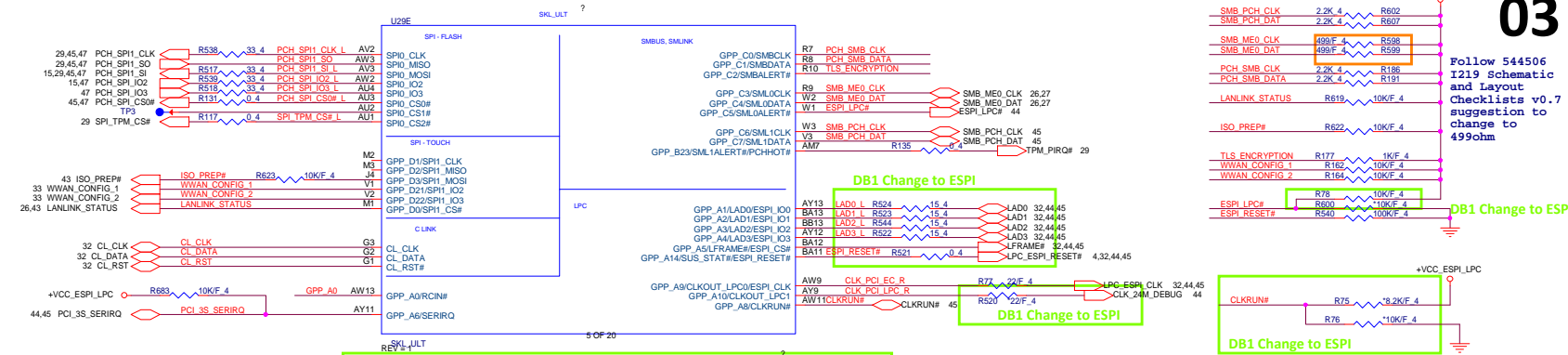


+VCCSTG 11,13,62  
 +VCCSFR 3,9,11,13,45,56,59,62  
 +3V 3,4,5,7,8,10,15,19,20,21,24,27,28,37,38,39,40,44,45,48,49,56,62,64

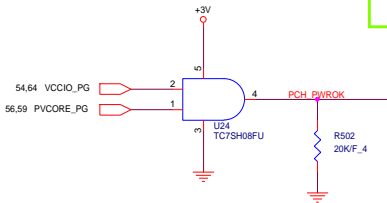
	PROJECT : Y0F		
	Quanta Computer Inc.		
Size Custom	Document Number	Rev	
NB5	SKYPAKE (MISC/JTAG)	1A	
Date: Tuesday, January 06, 2015	Sheet	2 of	67

03

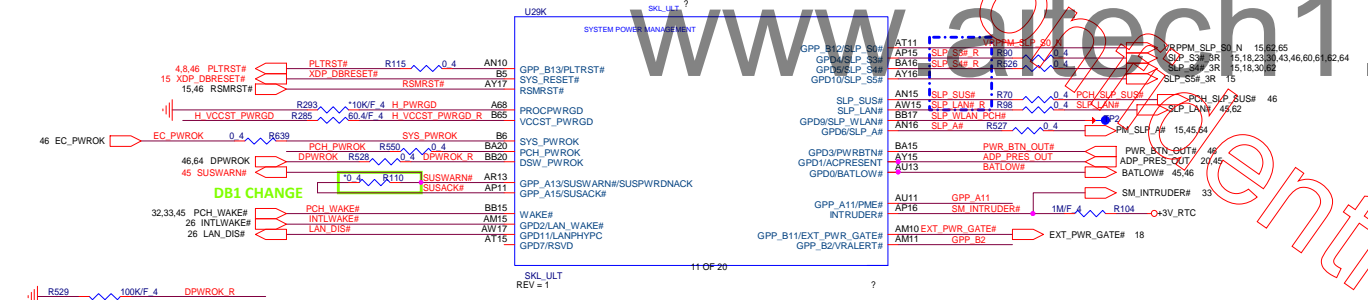
Follow 544506  
I219 Schematic  
and Layout  
Checklists v0.7  
suggestion to  
change to  
499ohm



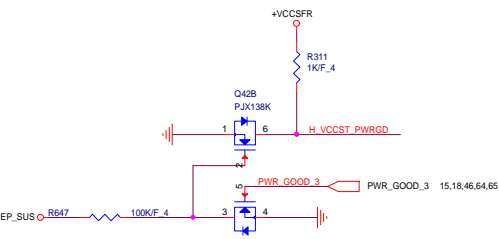
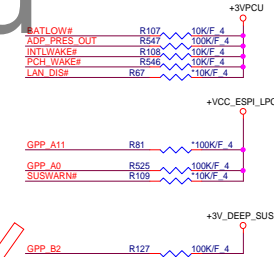
DB1 change to DNI, follow Nuvoton suggestion



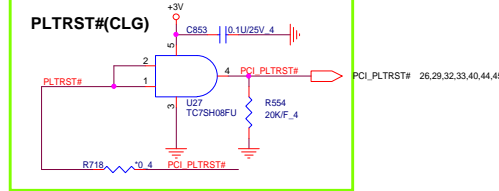
DDR/DOCK/XDP



PCH Pull-high/low(CLG)



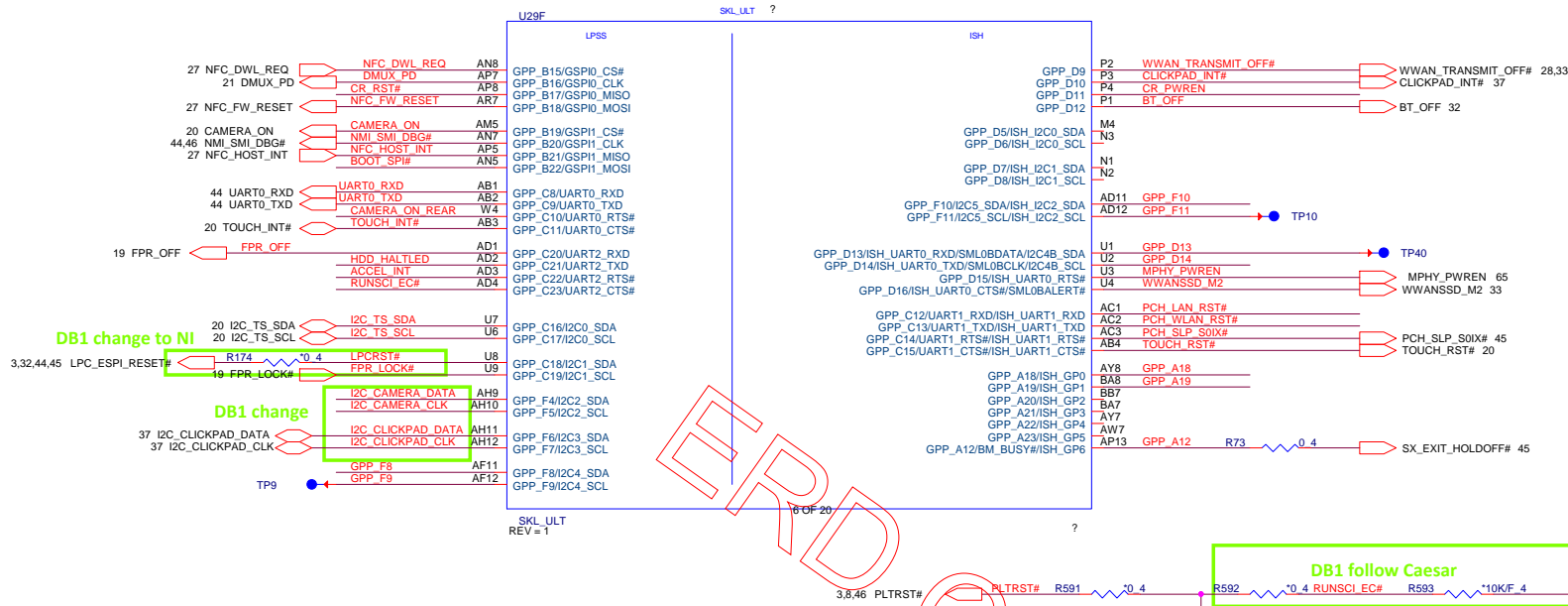
DB1 CHANGE



3V\_DEEP\_SUS 4,5,6,8,10,15,18,27,32,45,47,52,54,55,62,64,65  
3VPCU 10,15,27,28,32,33,35,36,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65  
3V\_ALW 9,18,35,49,50,53,62,63,64,65  
3V\_2.4,5,7,8,9,10,15,19,20,21,24,27,28,37,38,39,40,44,45,48,49,56,62,64  
+VCCSFR 2,8,11,13,45,56,62  
+1.2VSUS 6,13,16,17,51  
+3V\_RTC 9,10,33,45

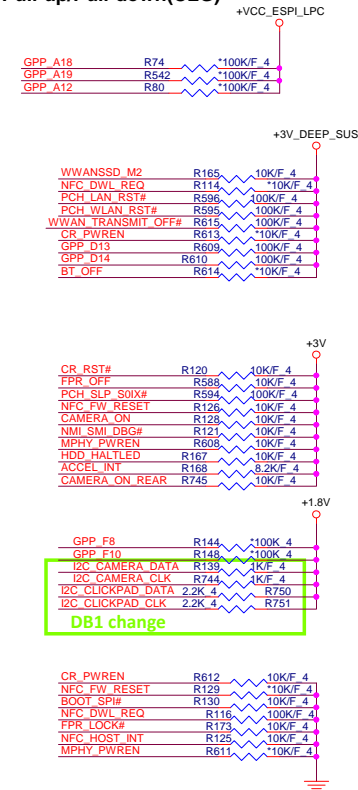
	LPC MODE	ESPI MODE
R524	0Ω	15Ω
R523	0Ω	15Ω
R544	0Ω	15Ω
R522	0Ω	15Ω
R521	UNINSTAL	INSTAL
R78	UNINSTAL	INSTAL
R600	INSTAL	UNINSTAL

## Skylake (GPIO)



Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "Top Swap" mode. (Default)</p> <p>1 = <b>Enable</b> "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>Software will not be able to clear the Top Swap bit until the system is rebooted.</li> <li>The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).</li> <li>This signal is in the primary well.</li> </ol>
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode. (Default)</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>

## GPIO Pull-up/Pull-down(CLG)



1.8V 5.8,11,24,37,64,65  
 +3VPCU 3,10,15,27,28,32,33,35,36,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65  
 +3V\_DEEP\_SUS 3,5,6,8,10,15,18,27,32,45,47,52,54,55,62,64,65  
 +3V 2,3,5,7,8,9,10,15,19,20,21,24,27,28,37,39,40,44,45,48,49,56,62,64





16 M\_A\_DQ[63:0]  
17 M\_B\_DQ[63:0]  
16 M\_A\_DQS[7:0]  
17 M\_B\_DQS[7:0]  
16 M\_A\_DQSP[7:0]  
17 M\_B\_DQSP[7:0]

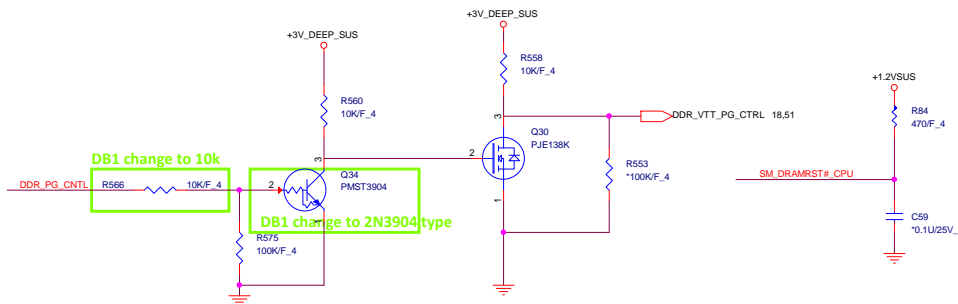
# SkyLake ULT Processor (DDR4-A)

# SkyLake ULT Processor (DDR4-B)

06



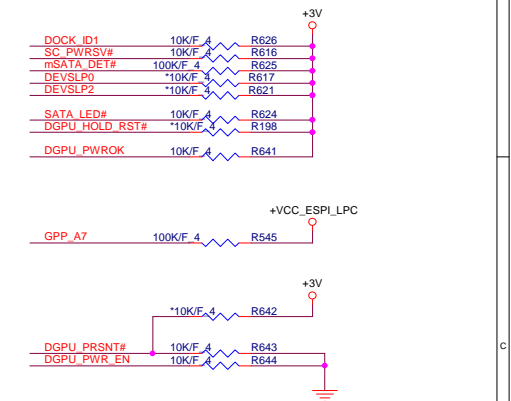
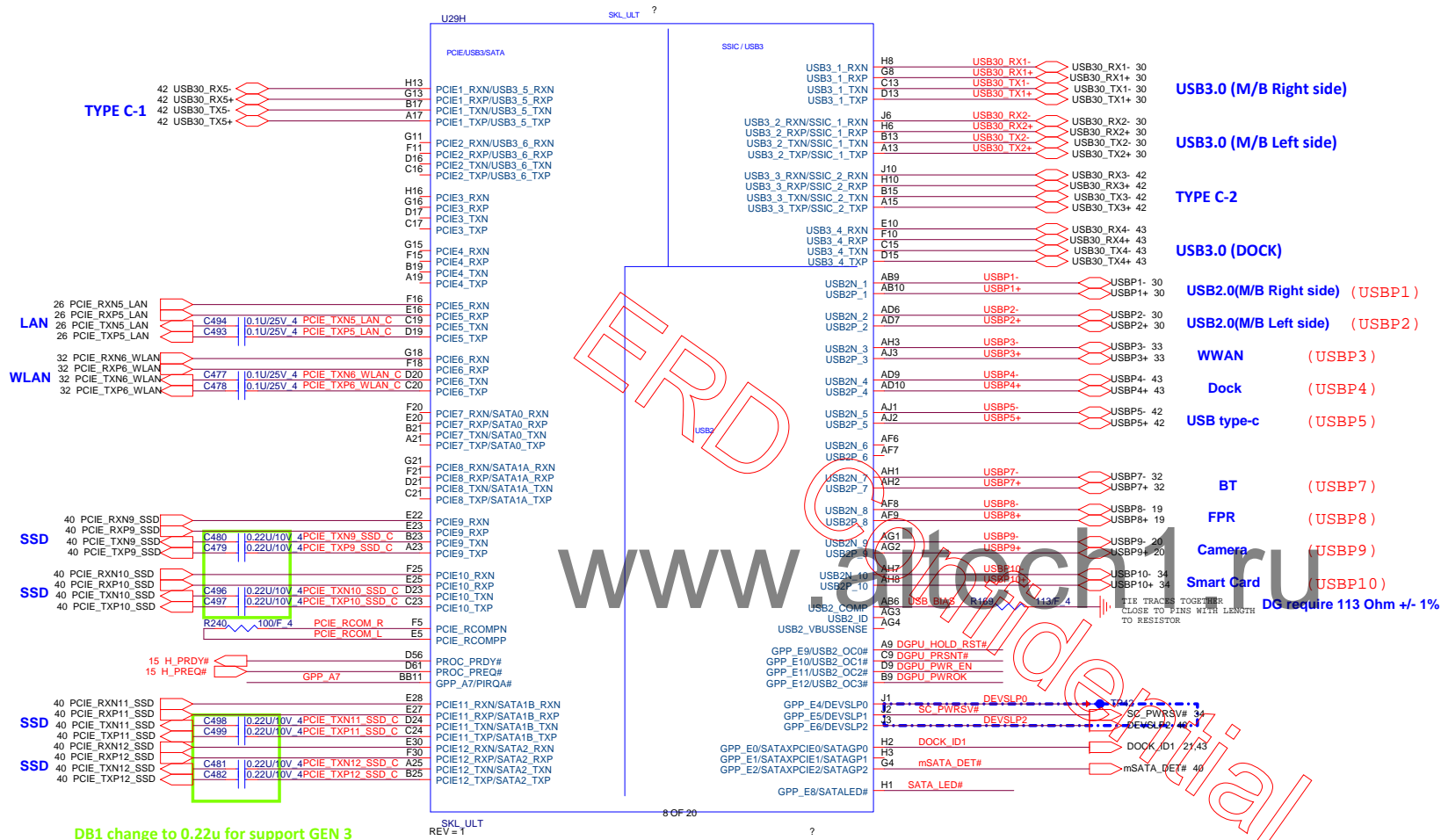
## DDR4 SODIMM ODT GENERATION

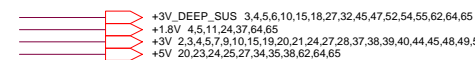
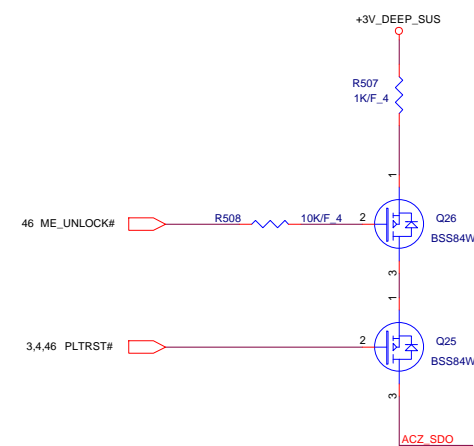
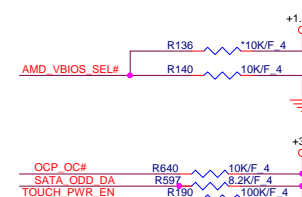
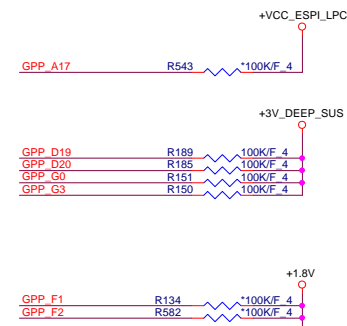
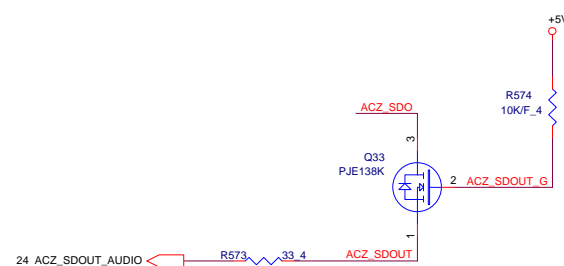
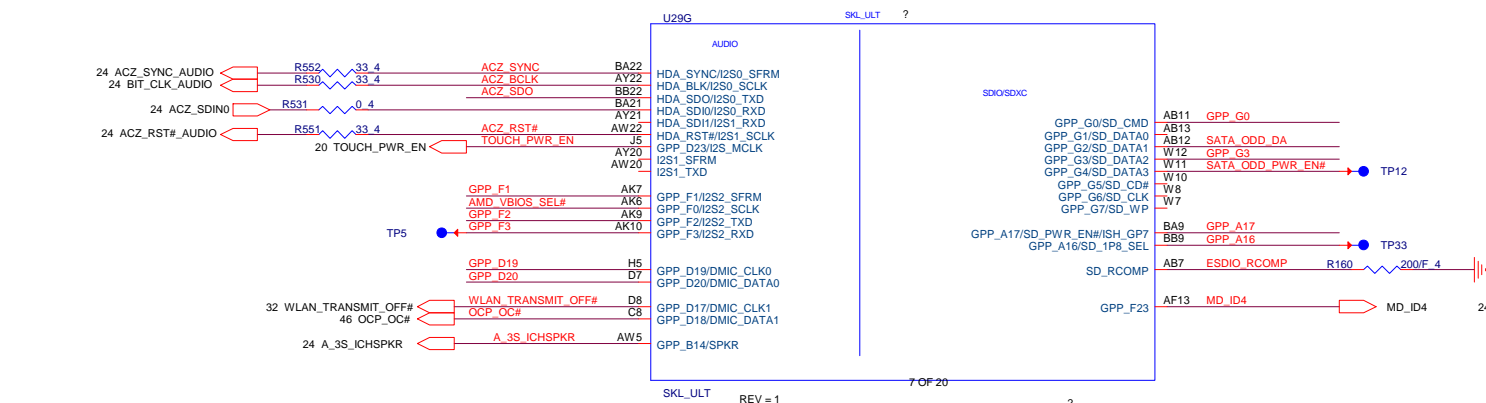


Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)			Max (mils) Length			R (Ω±1%) C (pF)	Notes	
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group	Byte	Region	Breakout			Total
RCOMP[0]	M	MS/SL/DSL	VSS	4	12-15					20	25		500		500	200	
RCOMP[1]	M	MS/SL/DSL	VSS	4	12-15					20	25		500		500	80.6	
RCOMP[2]	M	MS/SL/DSL	VSS	4	12-15					20	25		500		500	100	

PROJECT : YOF  
Quanta Computer Inc.

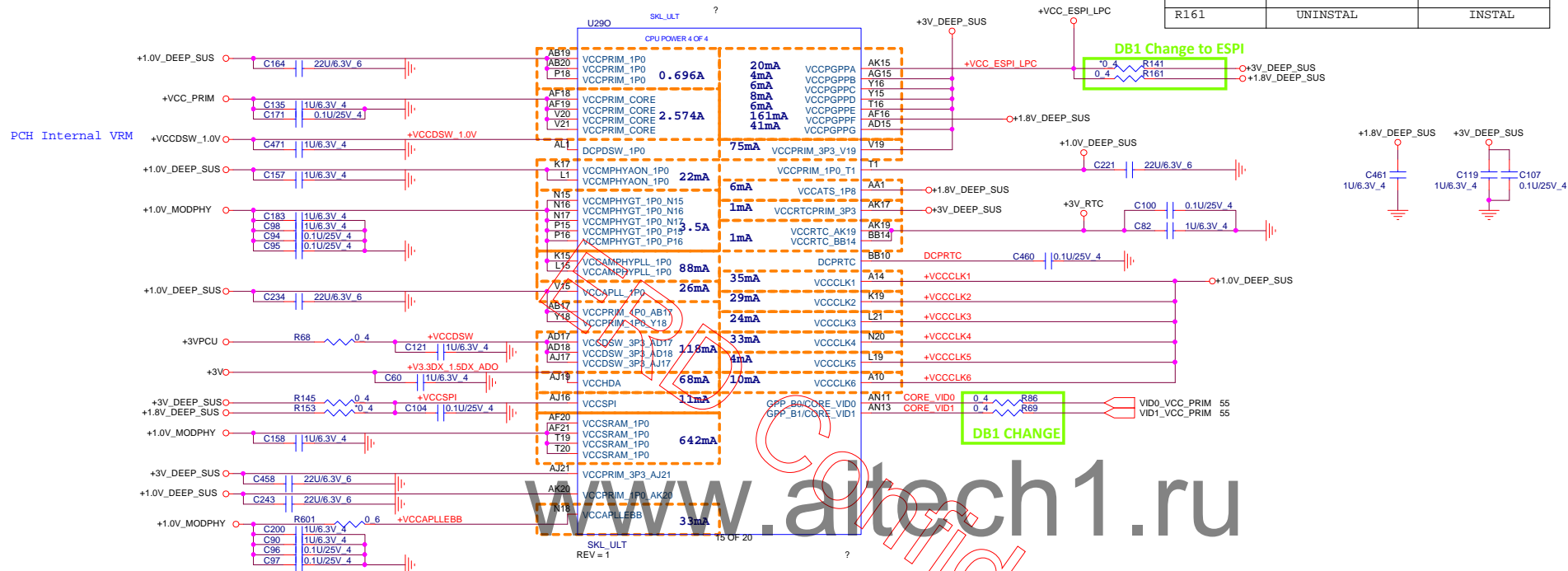
Size Custom	Document Number SKYPAKE (DDR4-A/B/I/F)	Rev 1A
Date: Tuesday, January 06, 2015	Sheet 6 of 67	








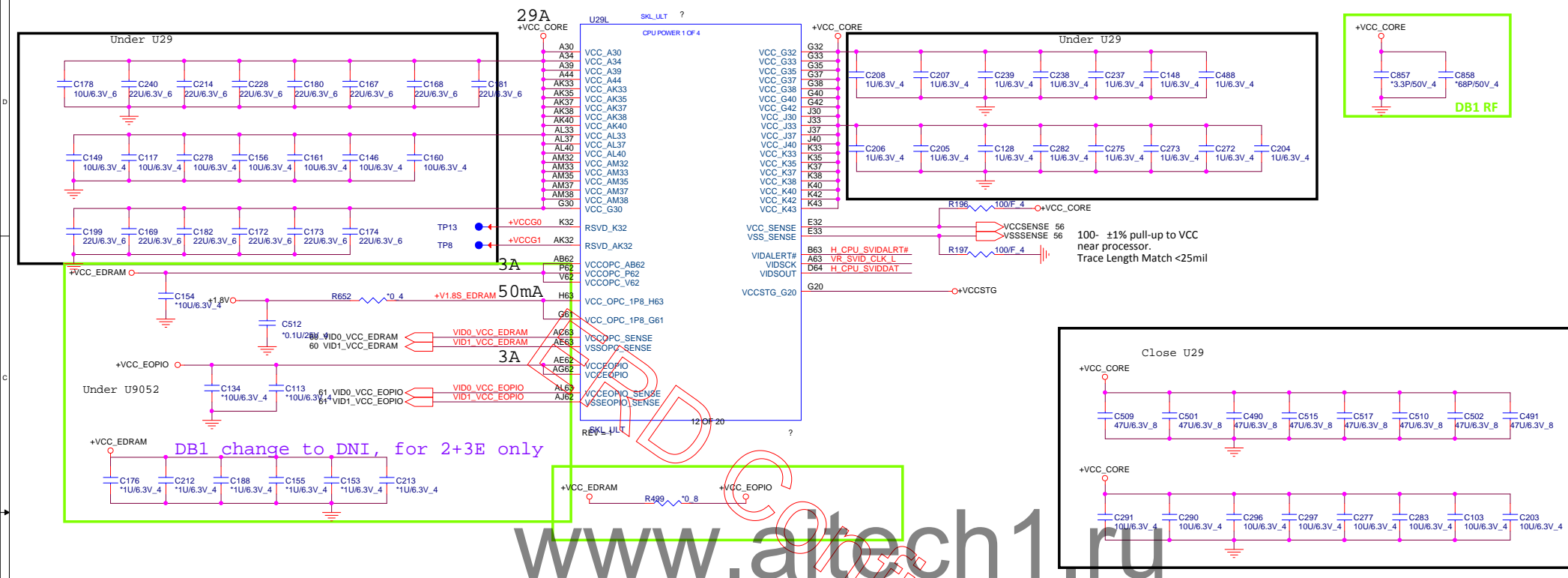
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R141	INSTAL	UNINSTAL
R161	UNINSTAL	INSTAL



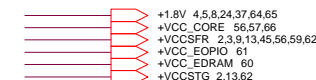
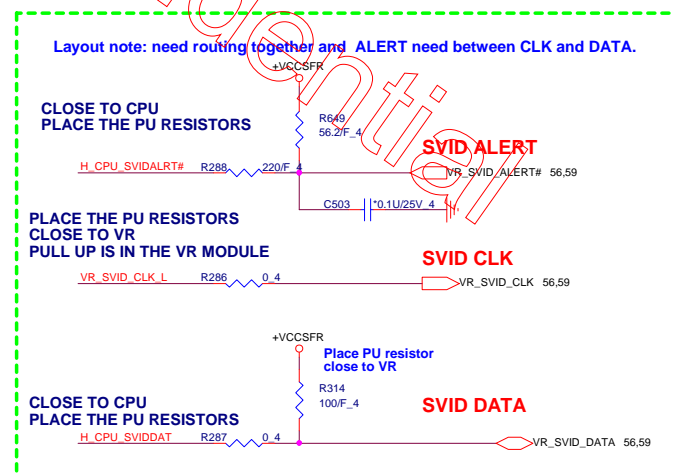
+3V\_DEEP\_SUS 3,4,5,6,8,15,18,27,32,45,47,52,54,55,62,64,65  
 +1.5V 21,52  
 +3VPCU 3,15,27,28,32,33,35,36,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65  
 +1.0V\_DEEP\_SUS 9,15,52,62,65  
 +VCC\_PRIM 55  
 +3V 2,3,4,5,7,8,9,15,19,20,21,24,27,28,37,38,39,40,44,45,48,49,56,62,64  
 +1.8V\_DEEP\_SUS 45,47,64,65

		<b>PROJECT : Y0F</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number SKYPAKE (PCH POWER)	Rev 1A	
Date: Tuesday, January 06, 2015	Sheet 10 of 67		

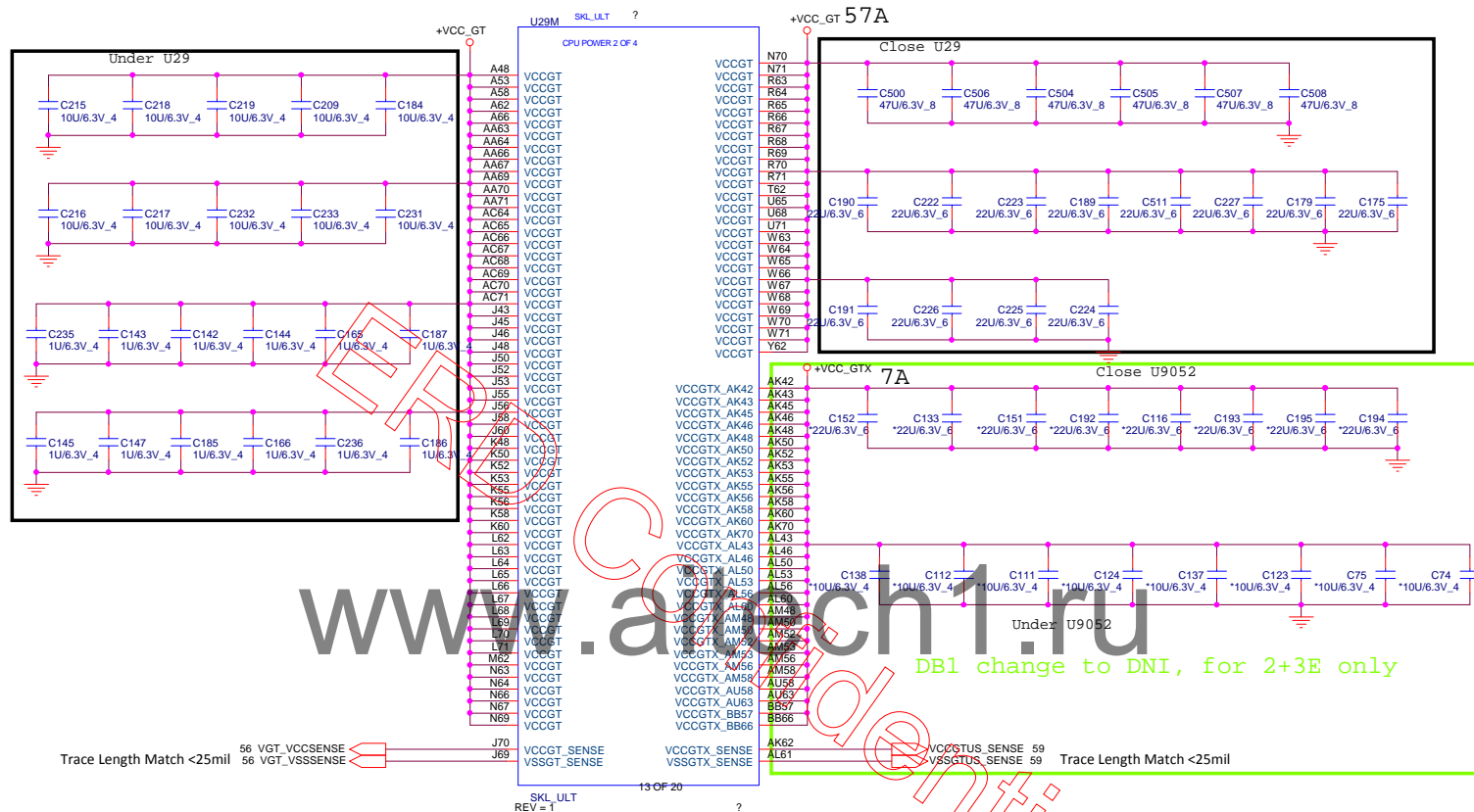




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

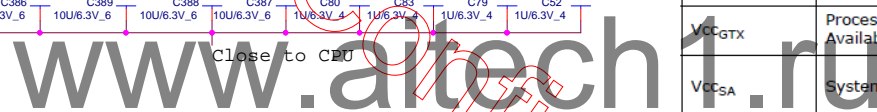








+VCC\_GT 56.58

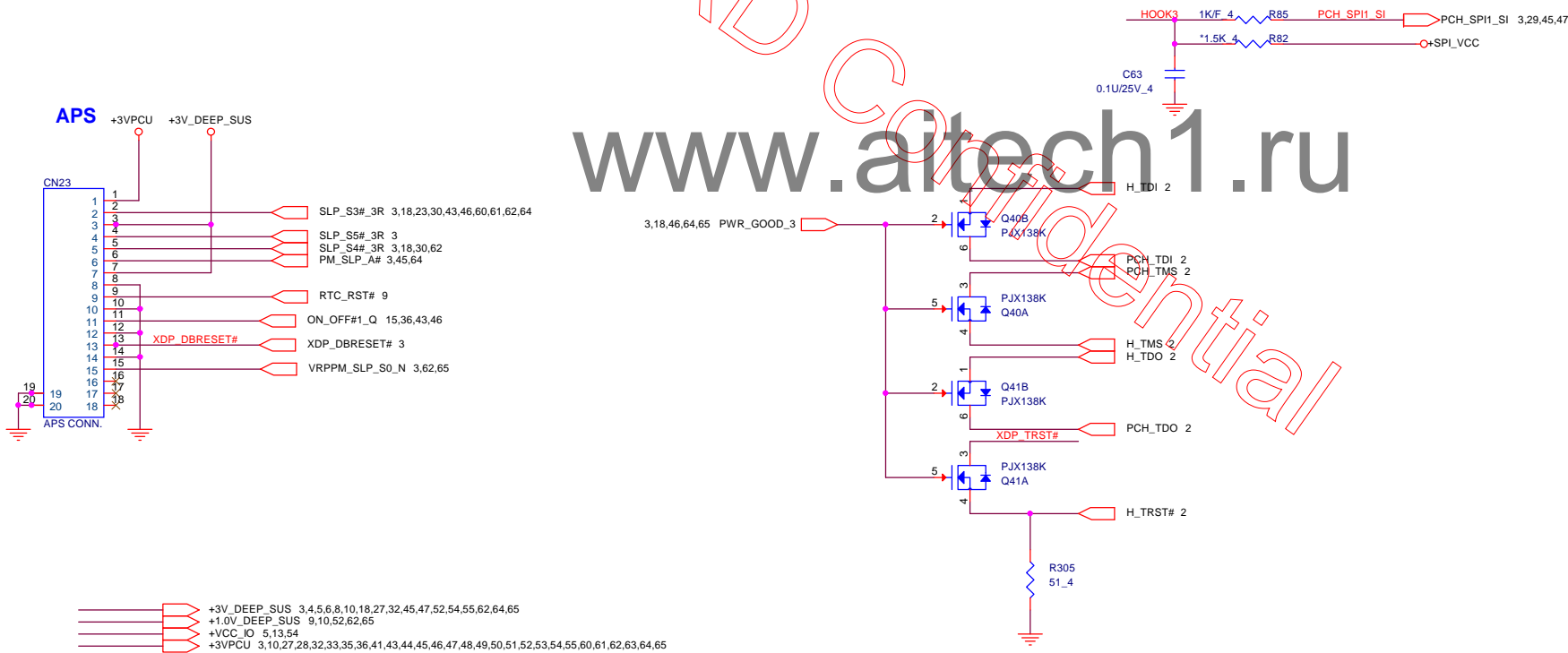
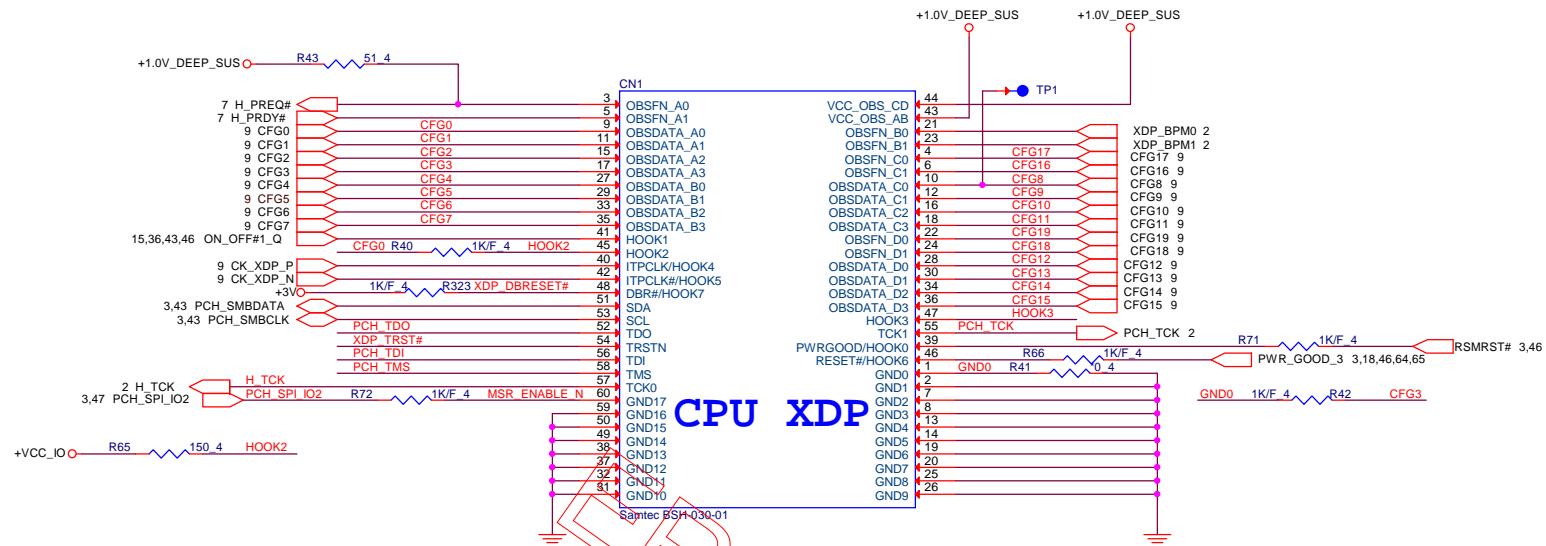
+VCC\_GTX 59

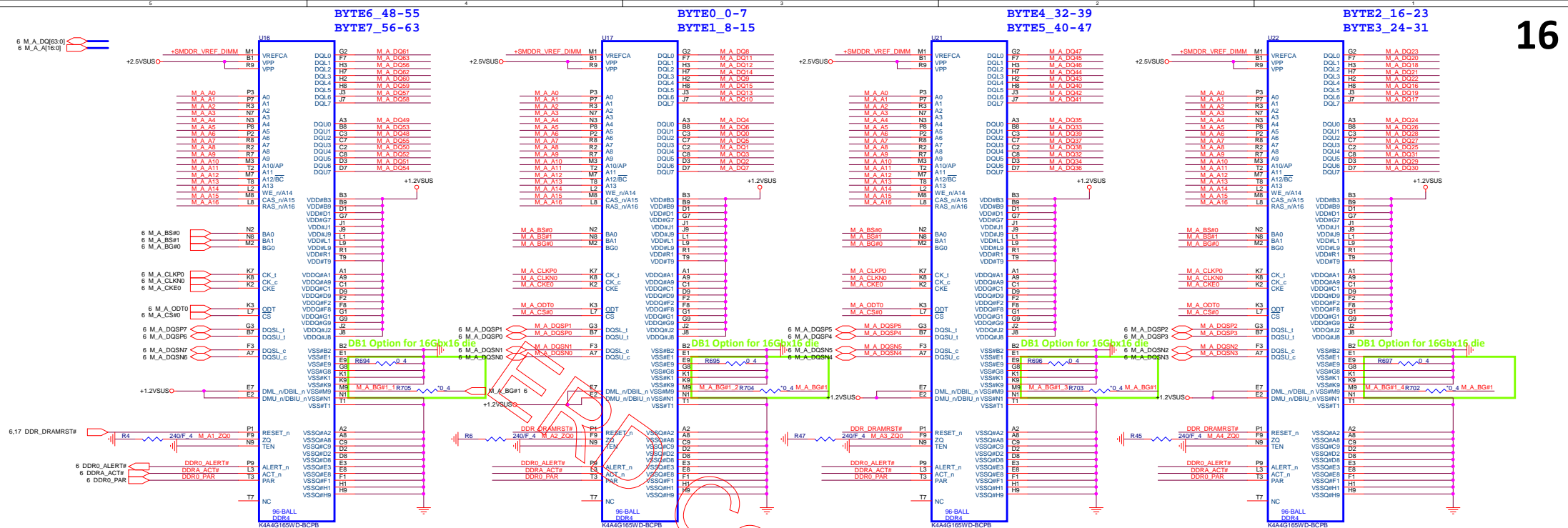



 +VCCSFR 2,3,9,11,45,56,59,62  
 +1.2VSUS 6,16,17,51  
 +VCCSTG 2,11,62  
 +VCC\_IO 5,15,54  
 +VCC\_SA 56,57,66

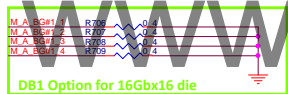
2

 <b>NB5</b>	<b>PROJECT : Y0F</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>SKYPAKE (GND)</b>	Rev <b>1A</b>
	Date: Tuesday, January 06, 2015	Sheet 14 of	67

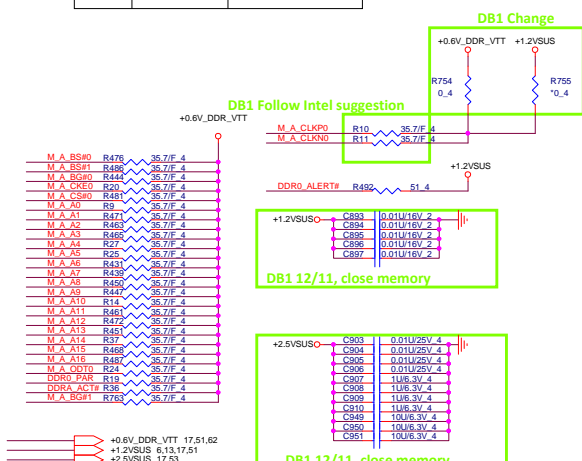




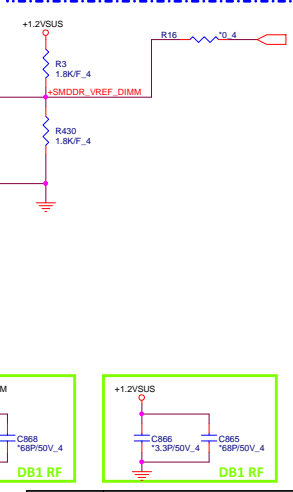
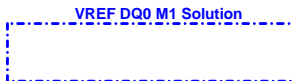
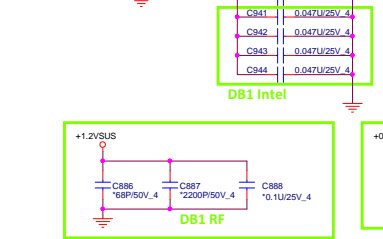
Vendor	P/N
Micron	
Elpida	
SAMSUNG	



DDP x16 & SDP x16 TABLE	
SDP x16	DDP x16
R694 0Ω CS00002JB38	240Ω CS12402FB03
R695 0Ω CS00002JB38	240Ω CS12402FB03
R696 0Ω CS00002JB38	240Ω CS12402FB03
R697 0Ω CS00002JB38	240Ω CS12402FB03
R702 UNINSTAL	UNINSTAL
R703 UNINSTAL	UNINSTAL
R704 UNINSTAL	UNINSTAL
R705 UNINSTAL	UNINSTAL
R706 UNINSTAL	UNINSTAL
R707 UNINSTAL	UNINSTAL
R708 UNINSTAL	UNINSTAL
R709 UNINSTAL	UNINSTAL



Place these Caps near Channel A  
1uF/10uF 4pcs on each side of connector

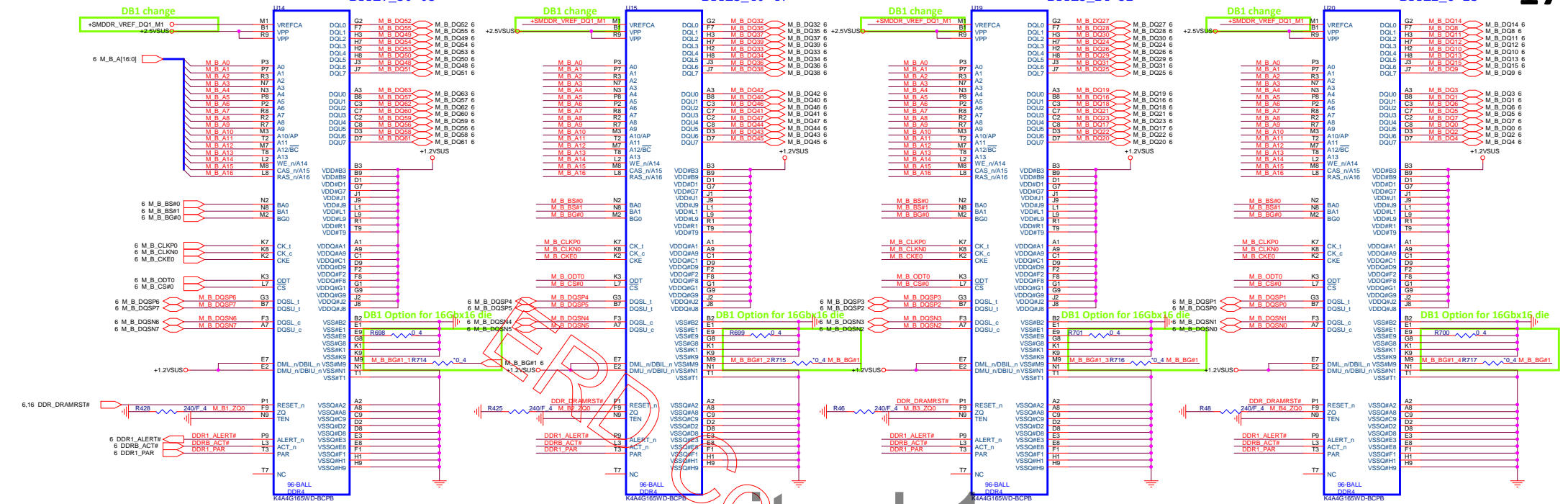


BYTE6\_48-55  
BYTE7\_56-63

BYTE4\_32-39  
BYTE5\_40-47

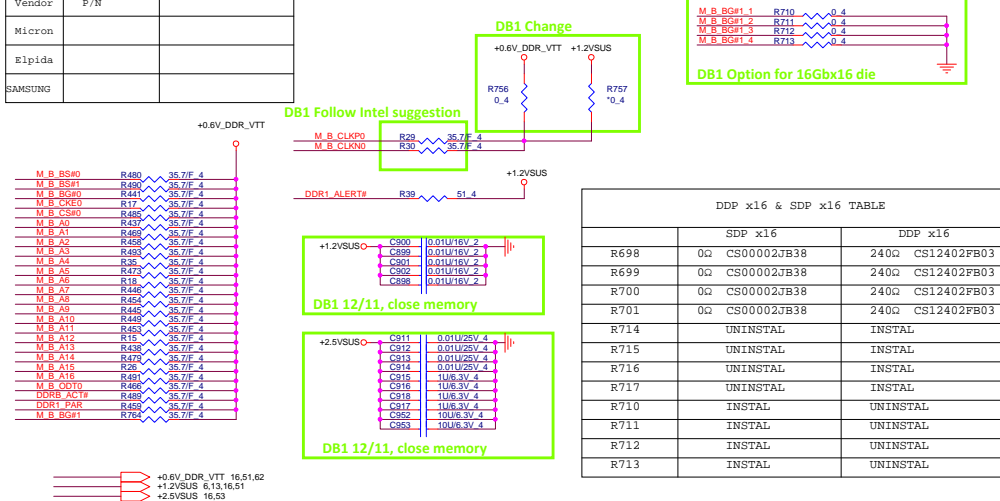
BYTE2\_16-23  
BYTE3\_24-31

BYTE0\_0-7  
BYTE1\_8-15

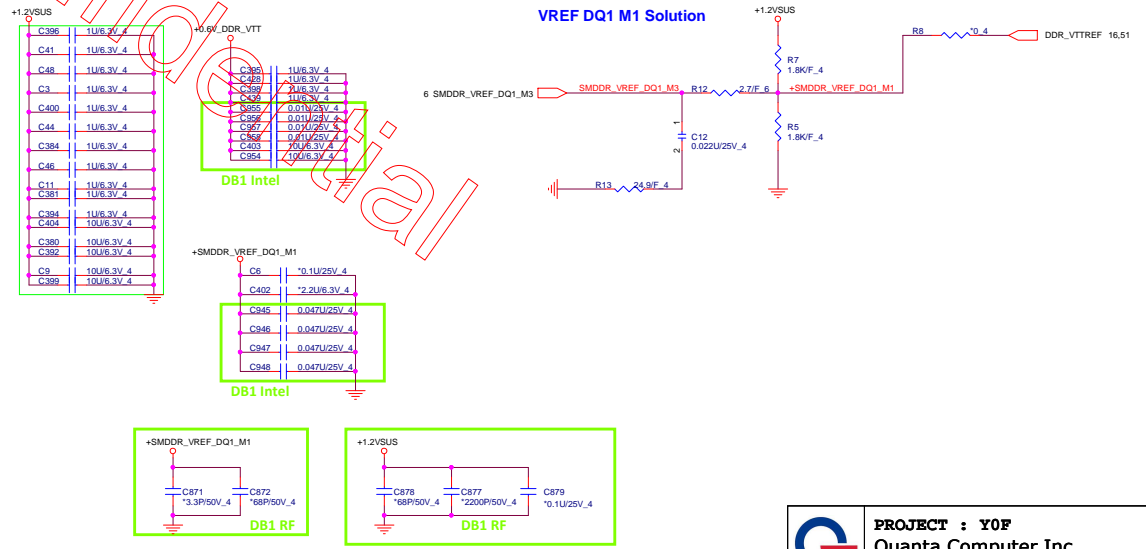


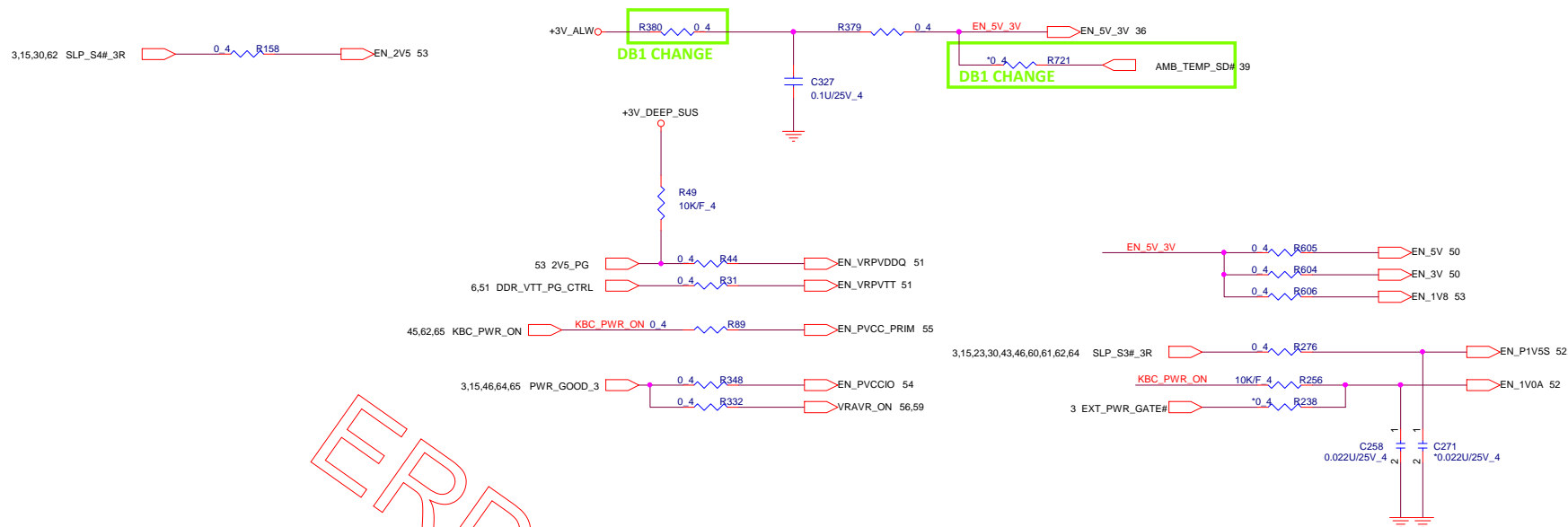
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Vendor	P/N	
Micron		
Elpida		
SAMSUNG		



DDP x16 & SDP x16 TABLE			
	SDP x16		DDP x16
R698	0Q	CS00002JB38	240Q CS12402FB03
R699	0Q	CS00002JB38	240Q CS12402FB03
R700	0Q	CS00002JB38	240Q CS12402FB03
R701	0Q	CS00002JB38	240Q CS12402FB03
R714		UNINSTAL	INSTAL
R715		UNINSTAL	INSTAL
R716		UNINSTAL	INSTAL
R717		UNINSTAL	INSTAL
R710		UNINSTAL	UNINSTAL
R711		INSTAL	UNINSTAL
R712		INSTAL	UNINSTAL
R713		INSTAL	UNINSTAL

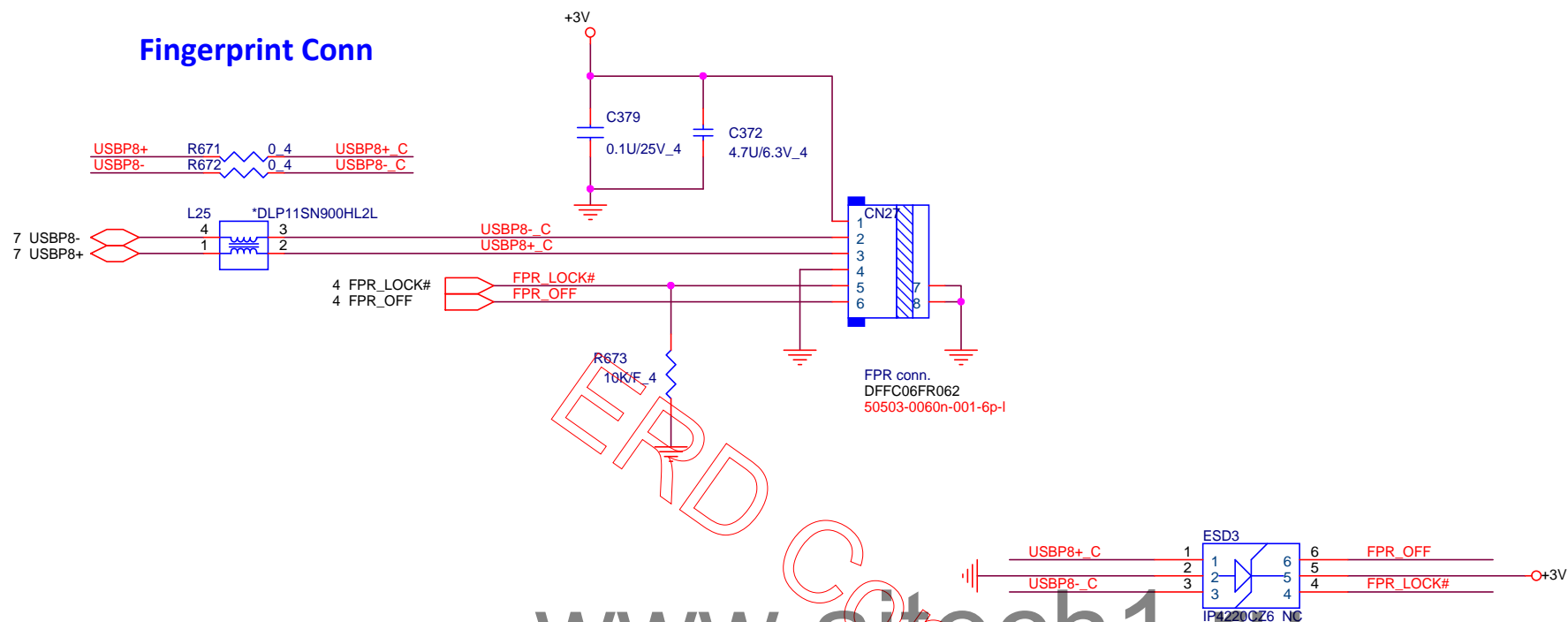





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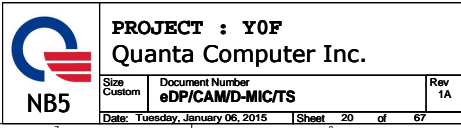
## Fingerprint Conn



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	PROJECT : Y0F		
	Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A	
	FPR		
Date: Thursday, January 08, 2015	Sheet 19 of 67		

# 20



3 Levels Input:  
L: Low  
H: High  
M: VDD33/2, connect both pull-up and pull-down resistors

MODE = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable

TMDS\_DDCBUF = L: DDC pass through  
= H: DDC active buffer  
= M: DDC pass through with 40 kohm pull up resistor

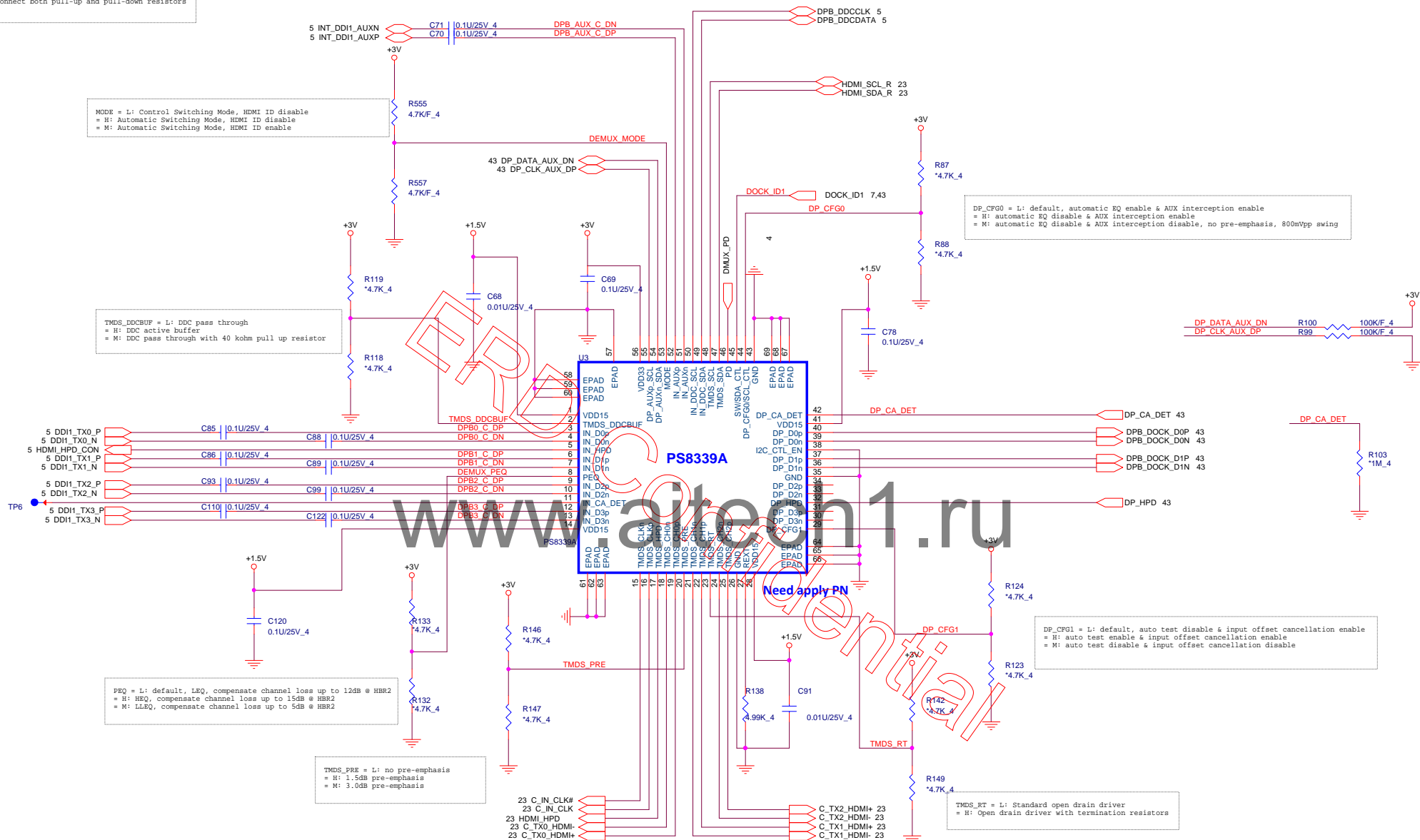
DP\_CFG0 = L: default, automatic EQ enable & AUX interception enable  
= H: automatic EQ disable & AUX interception enable  
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

DP\_CFG1 = L: default, auto test disable & input offset cancellation enable  
= H: auto test enable & input offset cancellation enable  
= M: auto test disable & input offset cancellation disable

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
= H: HEQ, compensate channel loss up to 15dB @ HBR2  
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

TMDS\_PRE = L: no pre-emphasis  
= H: 1.5dB pre-emphasis  
= M: 3.0dB pre-emphasis

TMDS\_RT = L: Standard open drain driver  
= H: Open drain driver with termination resistors



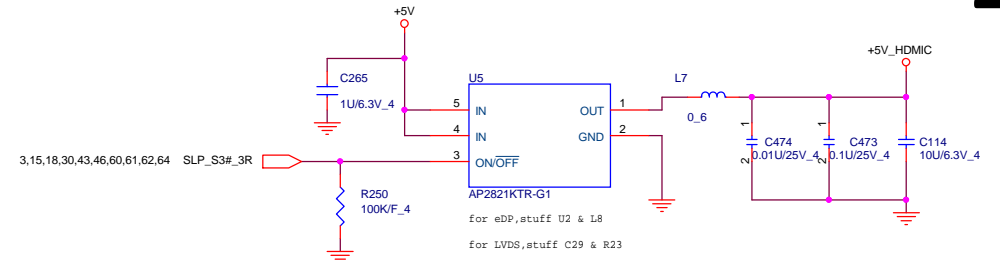
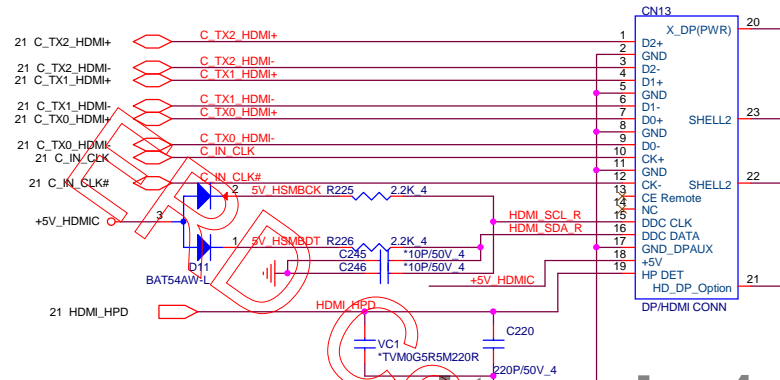
ERD  
www.altech1.ru  
Confidential

## EMI Solution

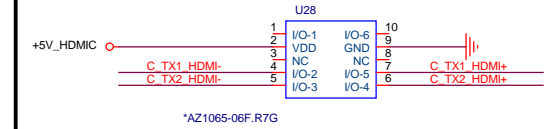
C_TX2_HDMI+	R157	*120/F_4	C_TX2_HDMI-
C_TX1_HDMI+	R163	*120/F_4	C_TX1_HDMI-
C_TX0_HDMI+	R170	*120/F_4	C_TX0_HDMI-
C_IN_CLK	R179	*120/F_4	C_IN_CLK#

21 HDMI\_SCL\_R HDMI\_SCL\_R  
21 HDMI\_SDA\_R HDMI\_SDA\_R

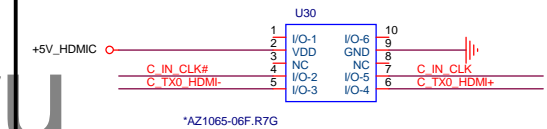
+5V\_HDMIC  
C136  
\*0.01U/16V\_4  
for EMI request



ESD chip, reserve



ESD chip, reserve



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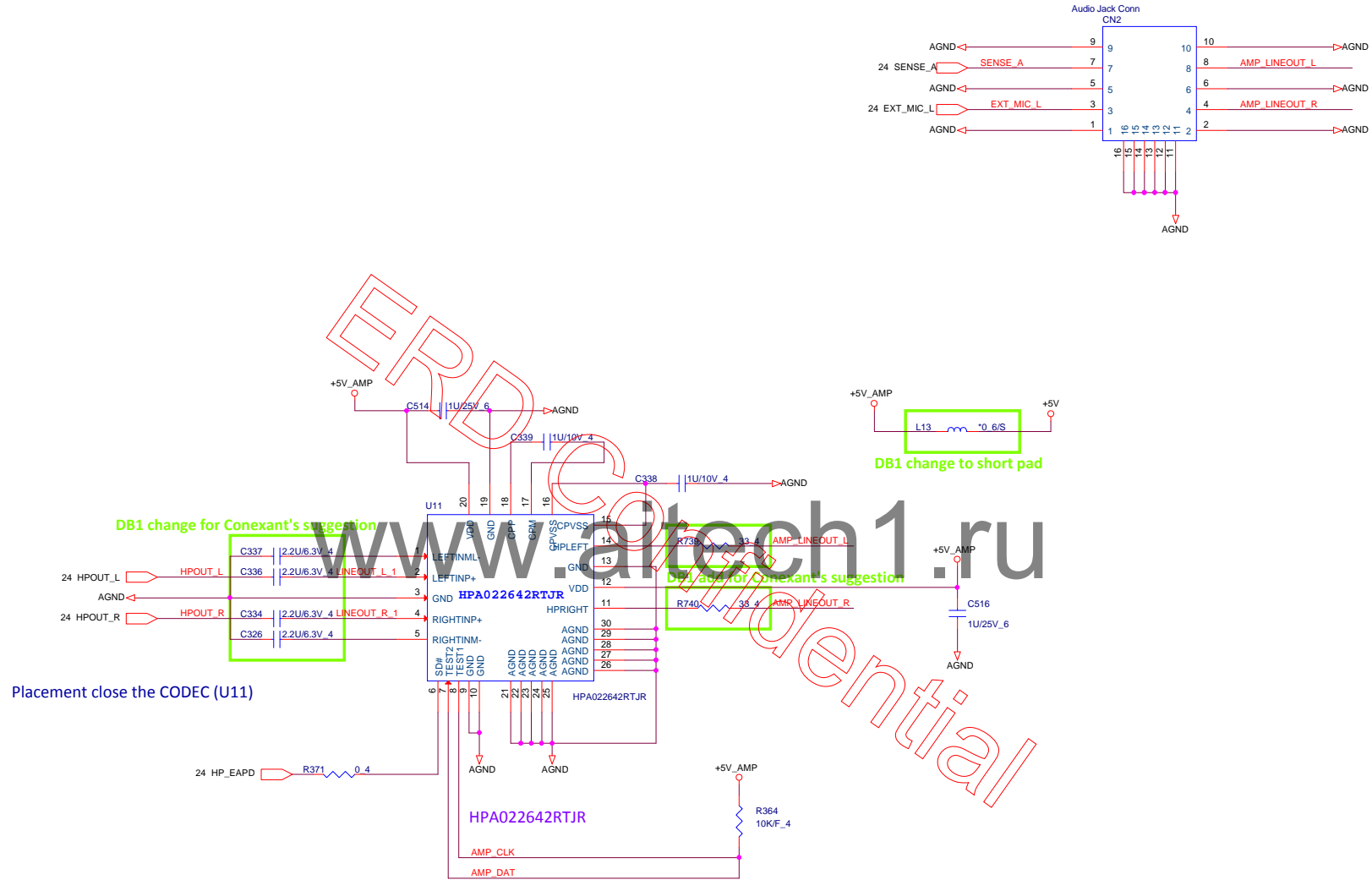


PROJECT : Y0F  
Quanta Computer Inc.

Size Custom	Document Number HDMI CONNECTOR	Rev 1A
Date: Tuesday, January 06, 2015	Sheet 23 of 67	

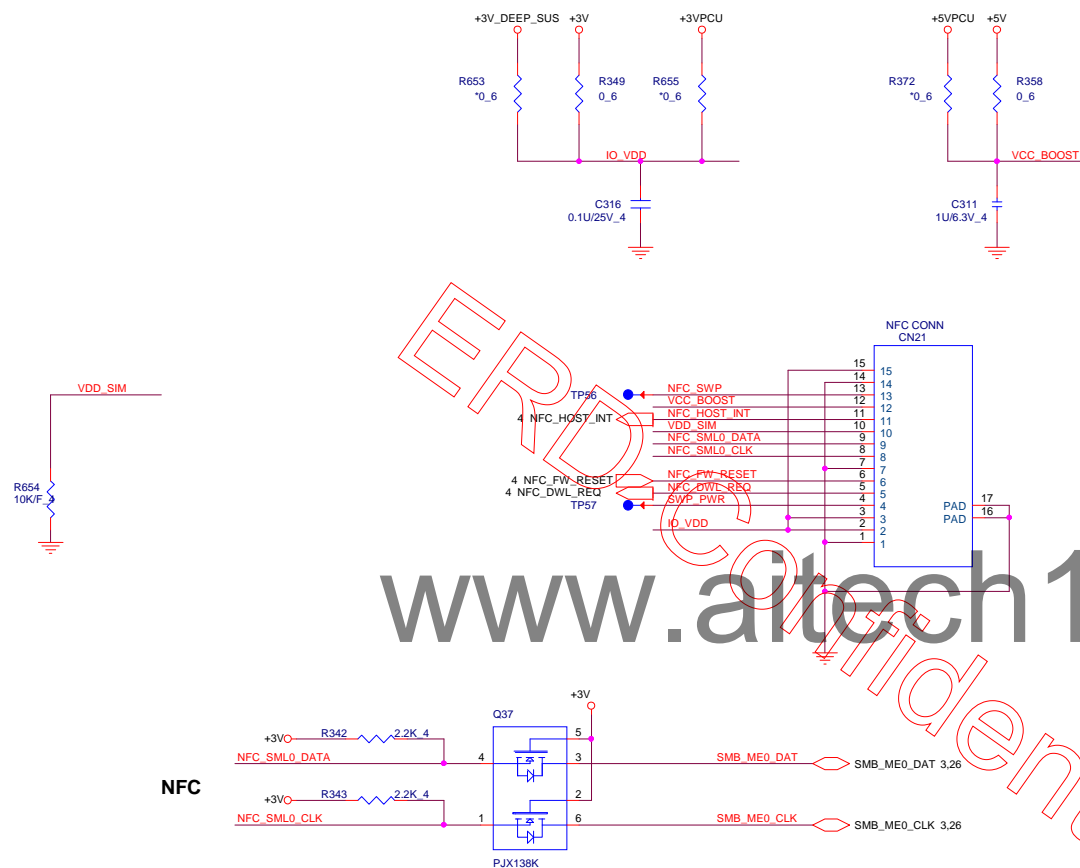


**Head Phone/MIC combo jack/AMP**

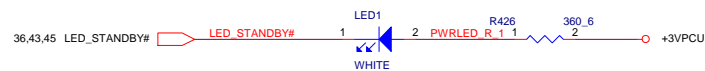




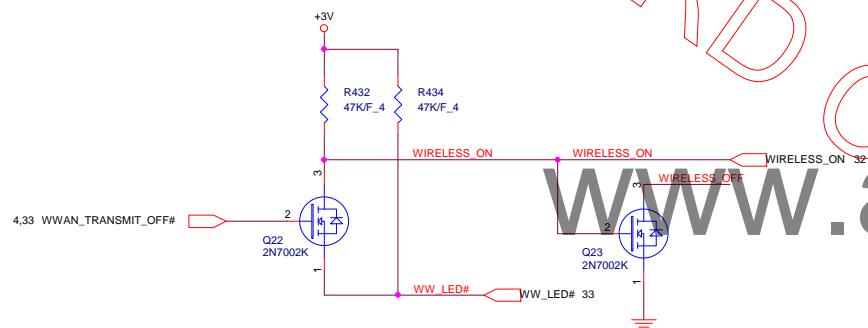
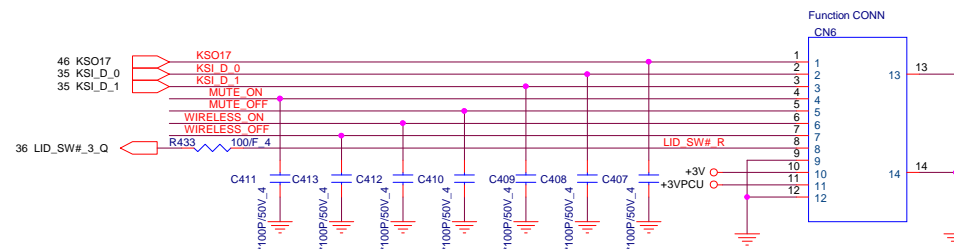
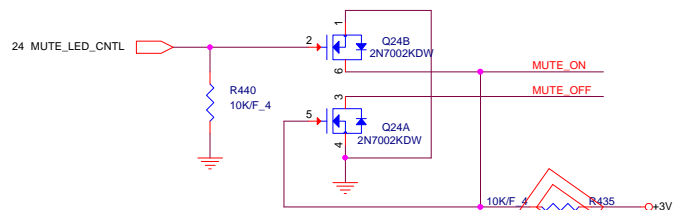
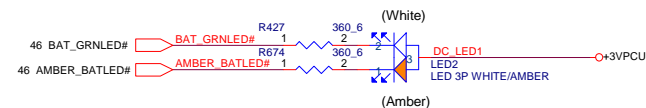





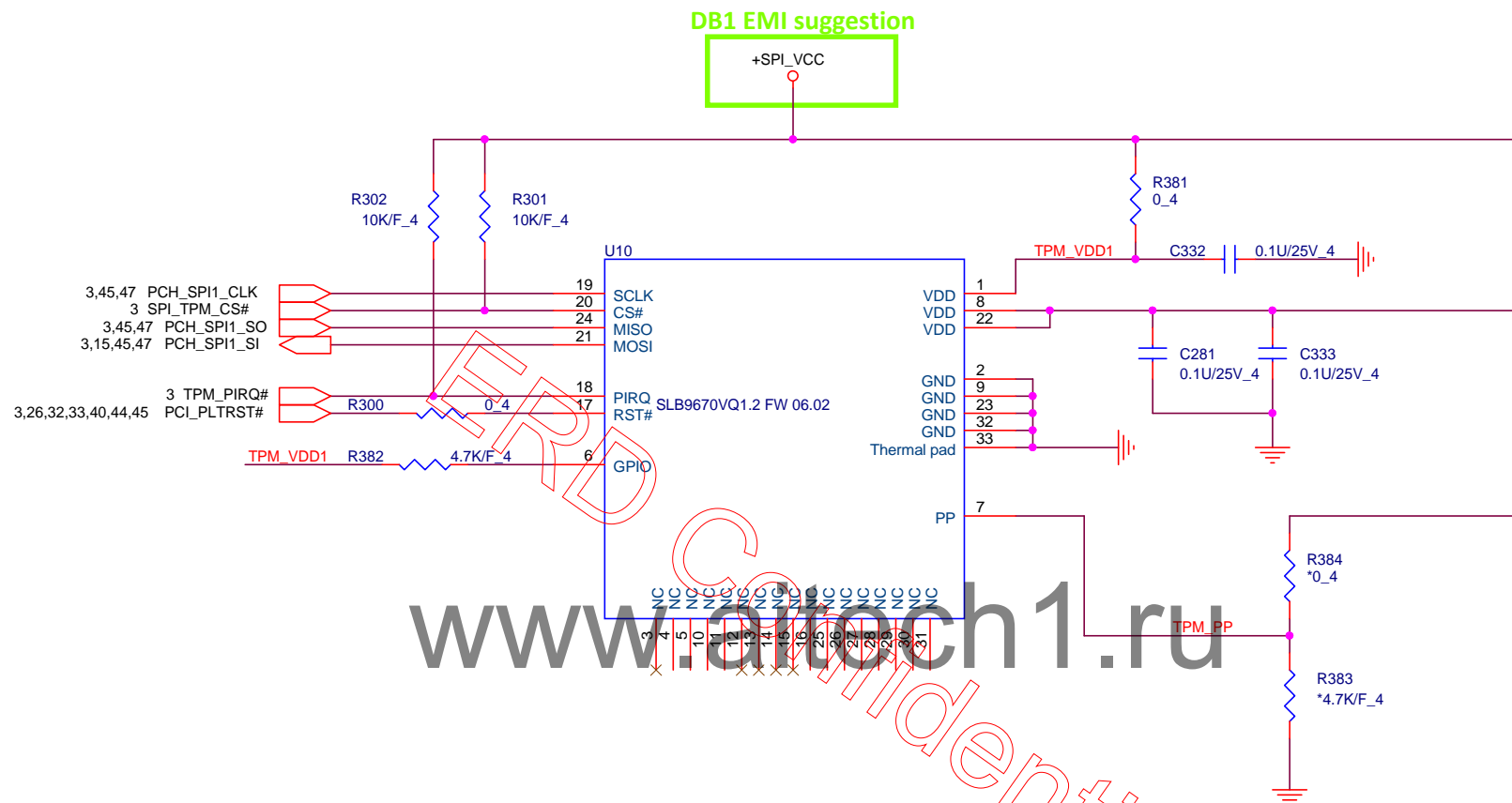
## PWR LED



## Battery LED



		<b>PROJECT : Y0F</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>LED &amp; Function Conn.</b>	Rev 1A	
Date: Tuesday, January 06, 2015	Sheet 28 of 67		

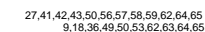




IC continuous output current is 2.5A

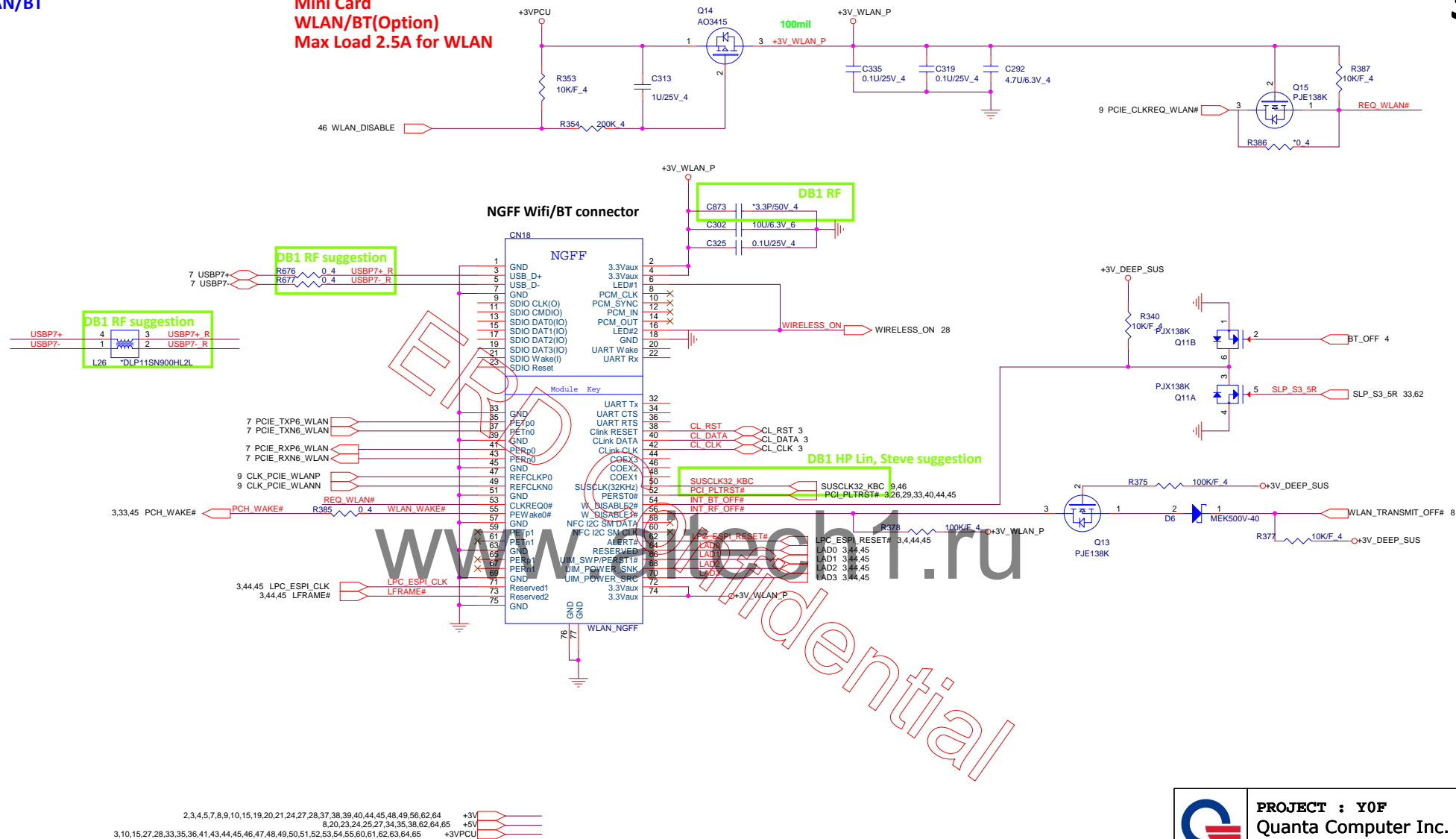


IC continuous output current is 2.5A




ERD  
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Confidential

Mini Card  
WLAN/BT(Optional)  
Max Load 2.5A for WLAN

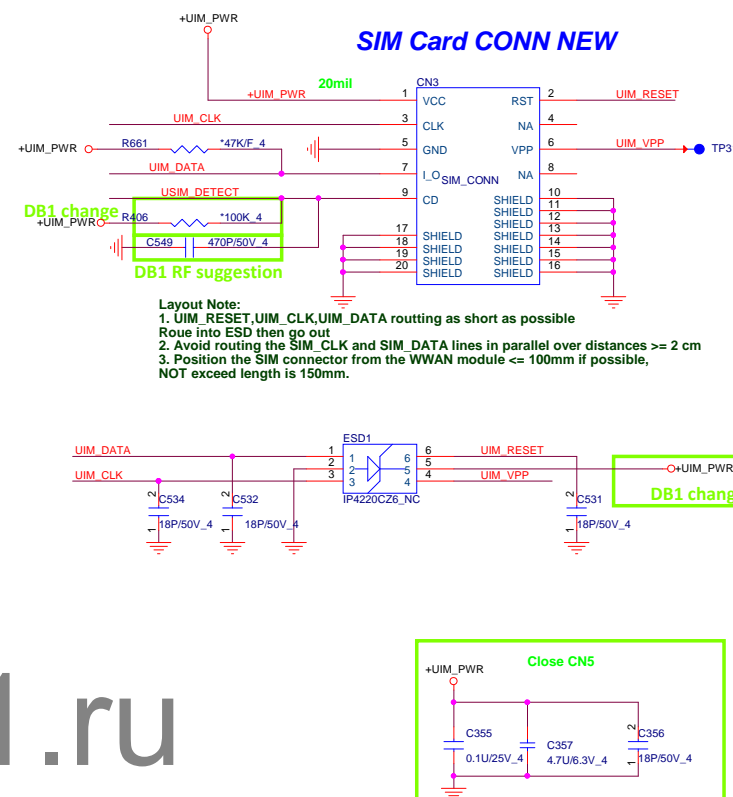


2,3,4,5,7,8,9,10,15,19,20,21,24,27,28,37,38,39,40,44,45,48,49,56,62,64  
8,20,23,24,25,27,34,35,38,62,64,65  
3,10,15,27,28,33,35,36,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65

+3V  
+5V  
+3VPCU

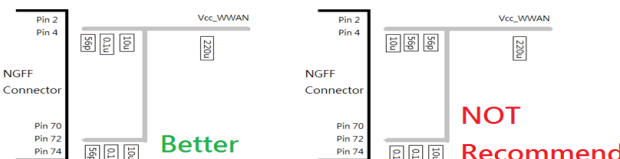
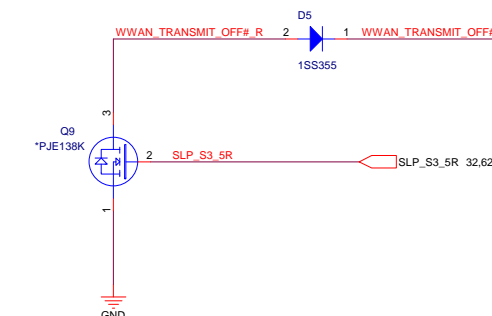
 NB5	PROJECT : Y0F Quanta Computer Inc.		
	Size Custom	Document Number NGFF WLAN/BT	Rev 1A
	Date: Tuesday, January 06, 2015	Sheet	32 of 67



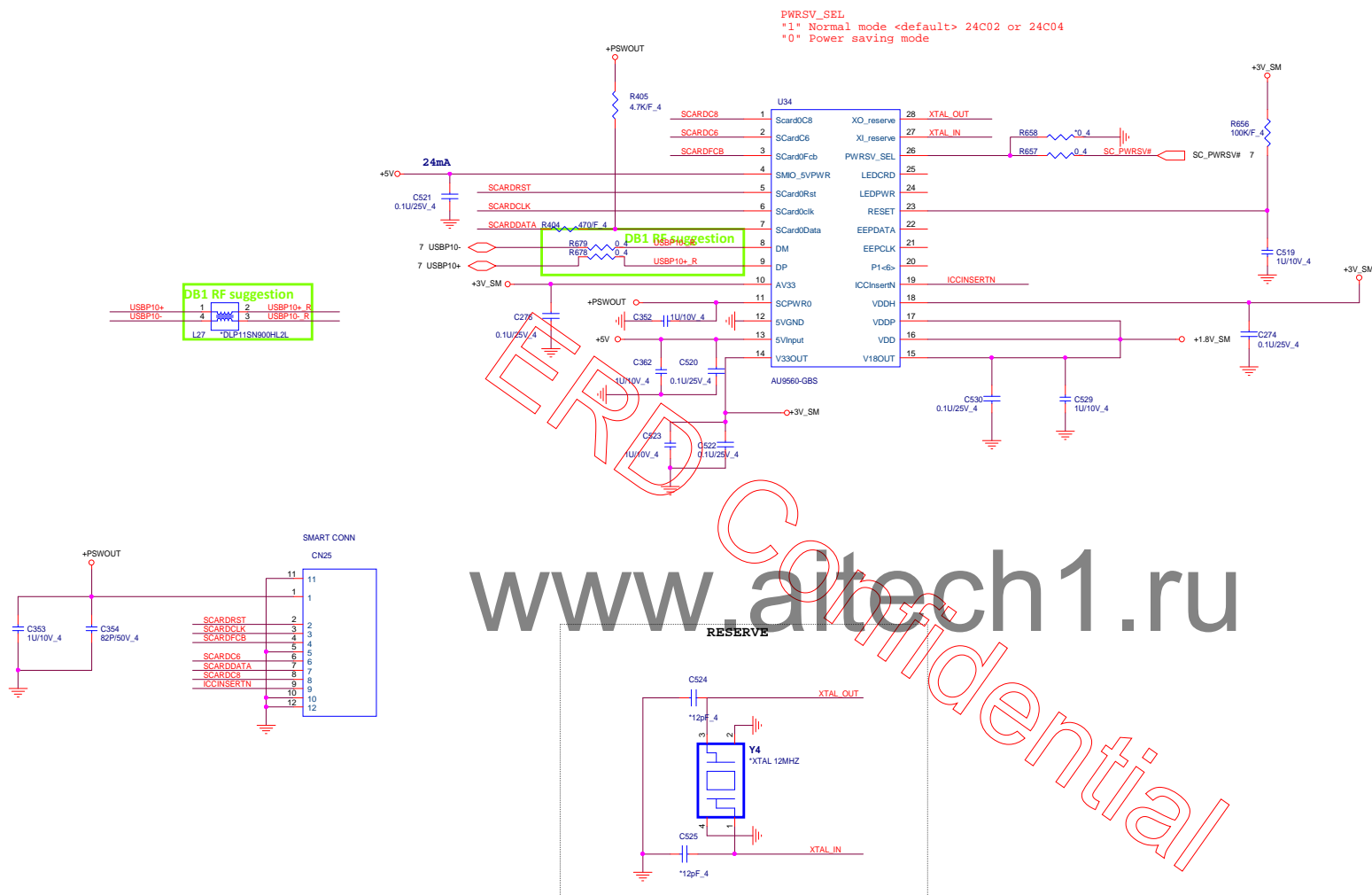


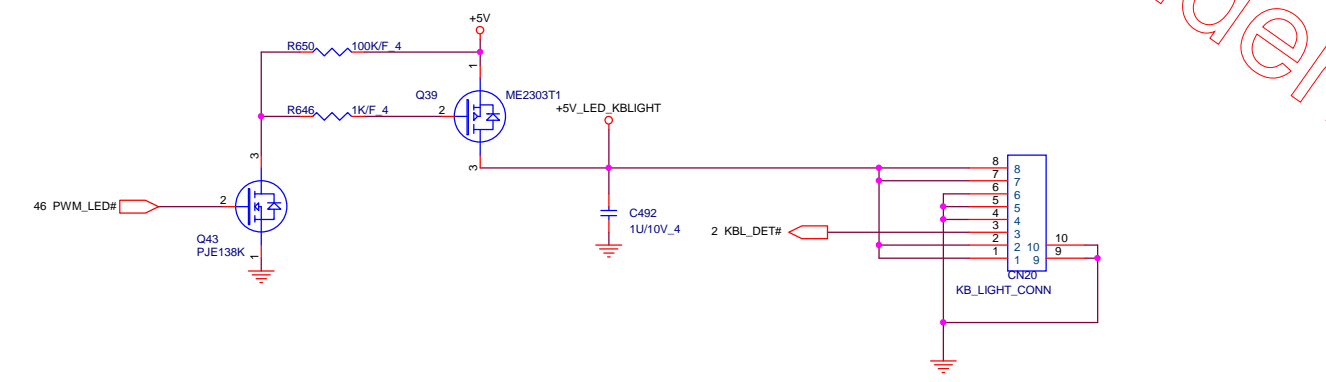
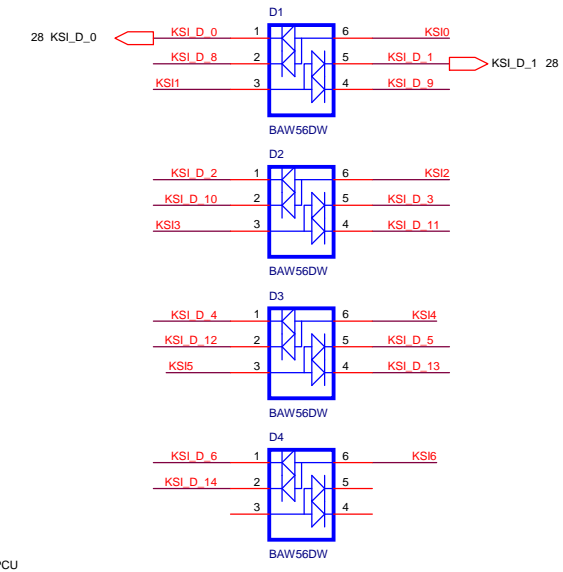
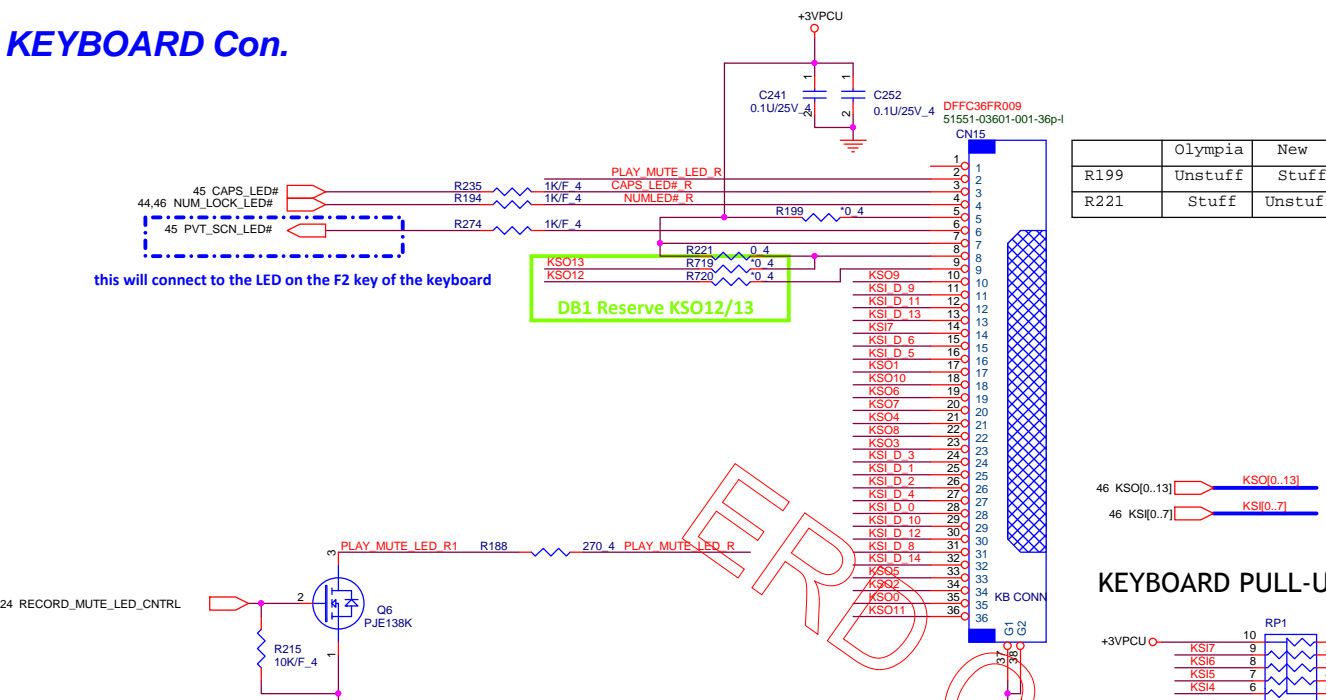
### Trace Length and Routing

- | ↕          | M.2 Pinout↕       | S0↕ | S3 – S5↕ |
|------------|-------------------|-----|----------|
| WWAN 3.3V↕ | 2, 4, 70, 72, 74↕ | On↕ | Off ↕    |



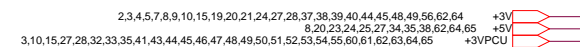
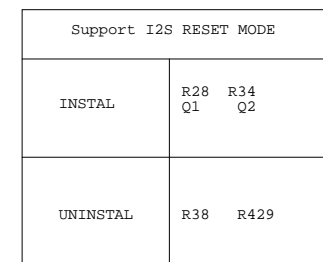
+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

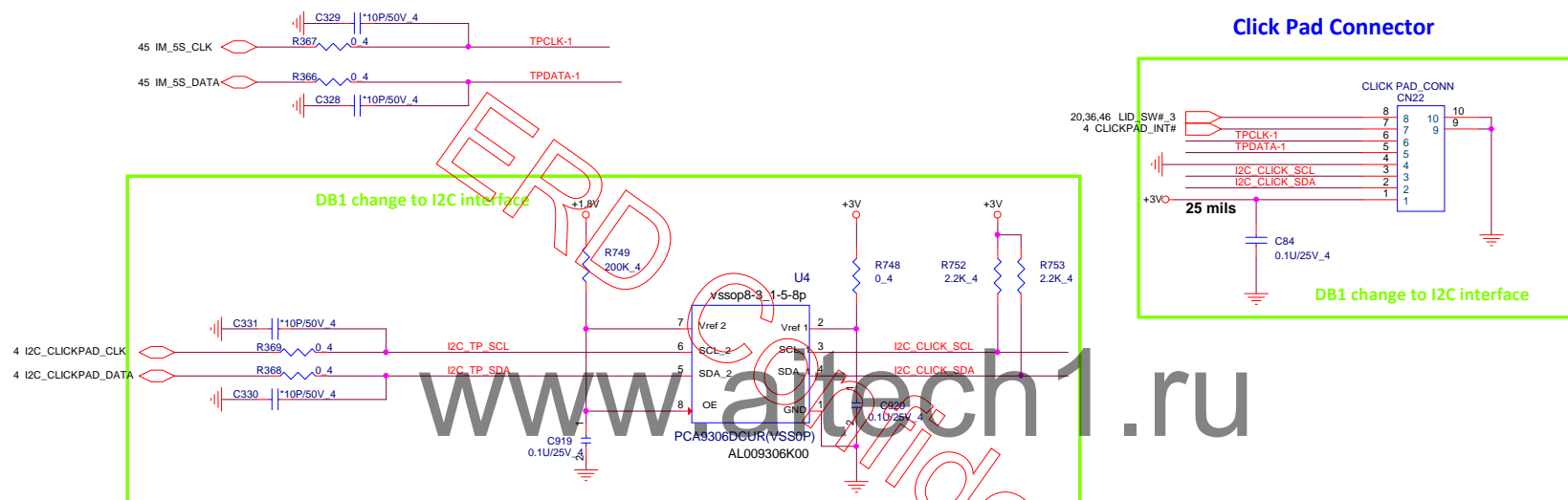




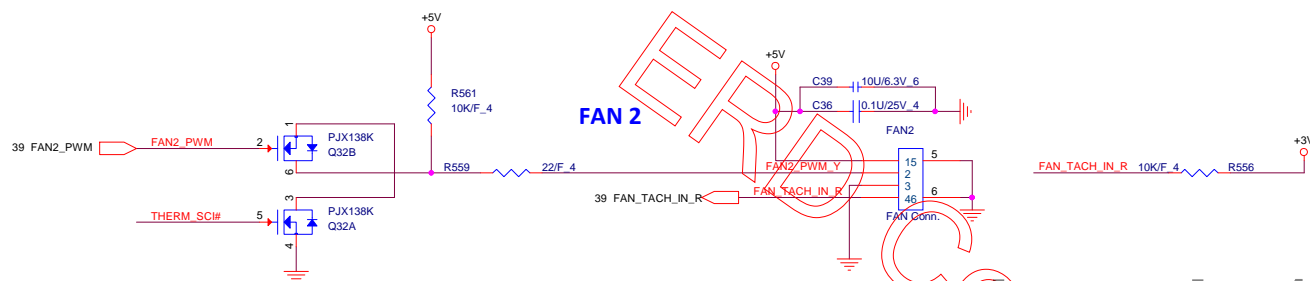
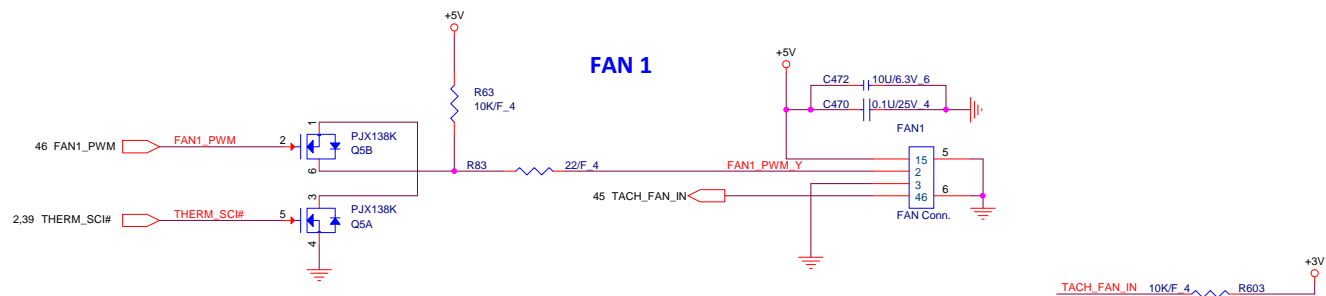
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2,3,4,5,7,8,9,10,15,19,20,21,24,27,28,37,38,39,40,44,45,48,49,56,62,64  
8,20,23,24,25,27,34,38,62,64,65 +5V  
3,10,15,27,28,32,33,36,41,43,44,45,46,47,48,49,50,51,52,53,54,55,60,61,62,63,64,65 +3VPCU





2,3,4,5,7,8,9,10,15,19,20,21,24,27,28,38,39,40,44,45,48,49,56,62,64  
4,5,8,11,24,64,65 +3V  
+1.8V



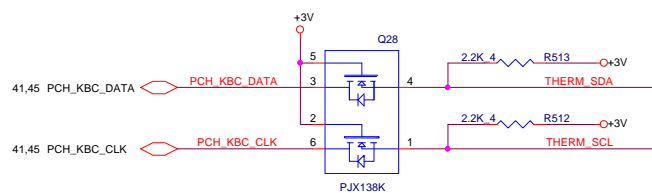
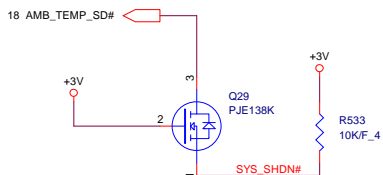
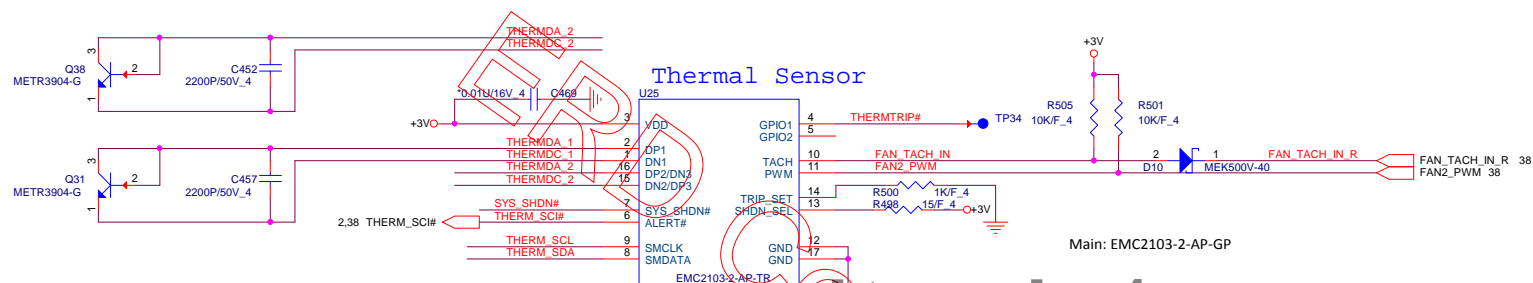
www.aitech1.ru

2,3,4,5,7,8,9,10,15,19,20,21,24,27,28,37,39,40,44,45,48,49,56,62,64  
8,20,23,24,25,27,34,35,62,64,65



**PROJECT : Y0F**  
**Quanta Computer Inc.**

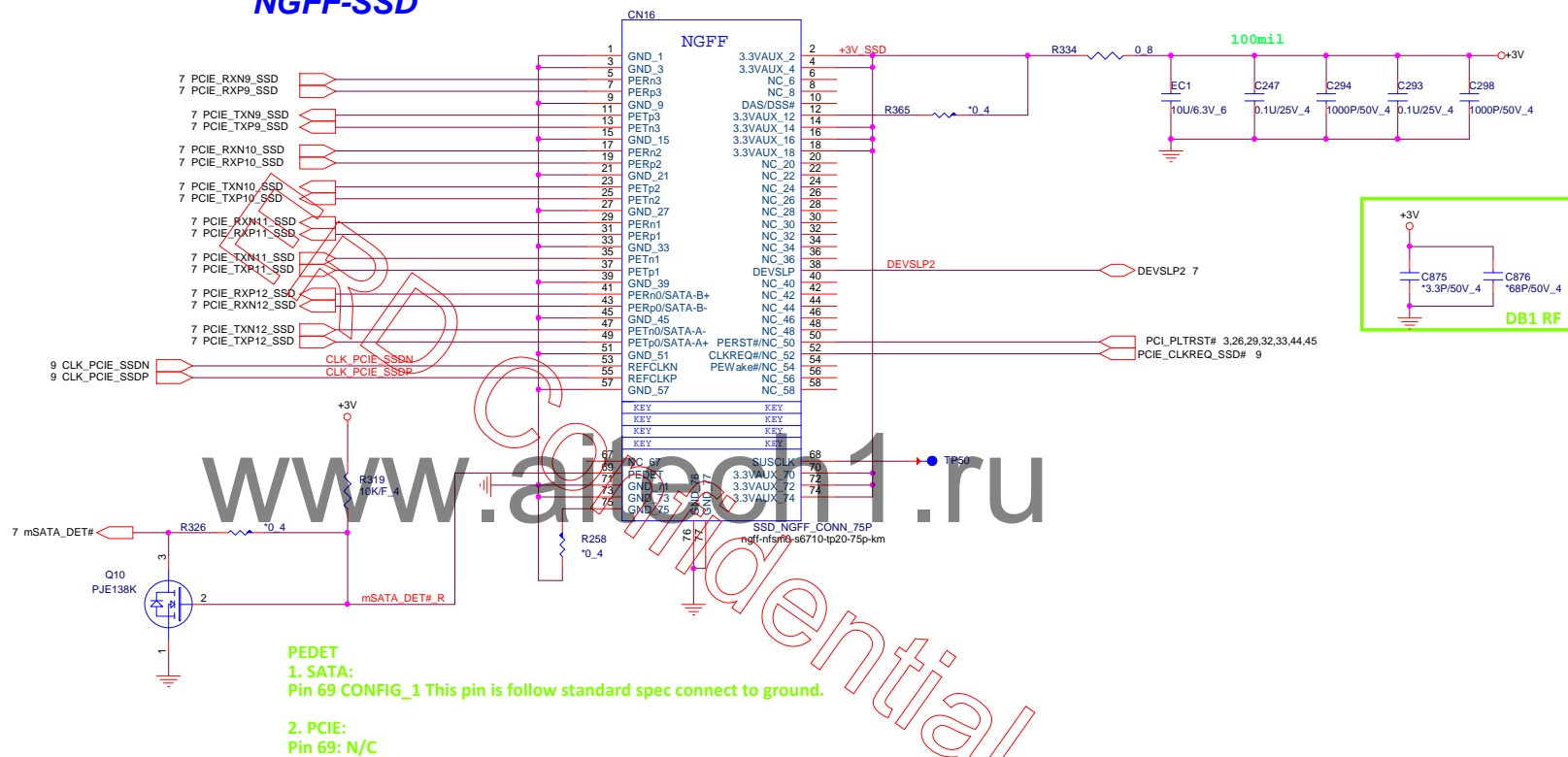
Size	Document Number	Rev
Custom	FAN	1A
Date: Tuesday, January 06, 2015	Sheet 36 of 67	



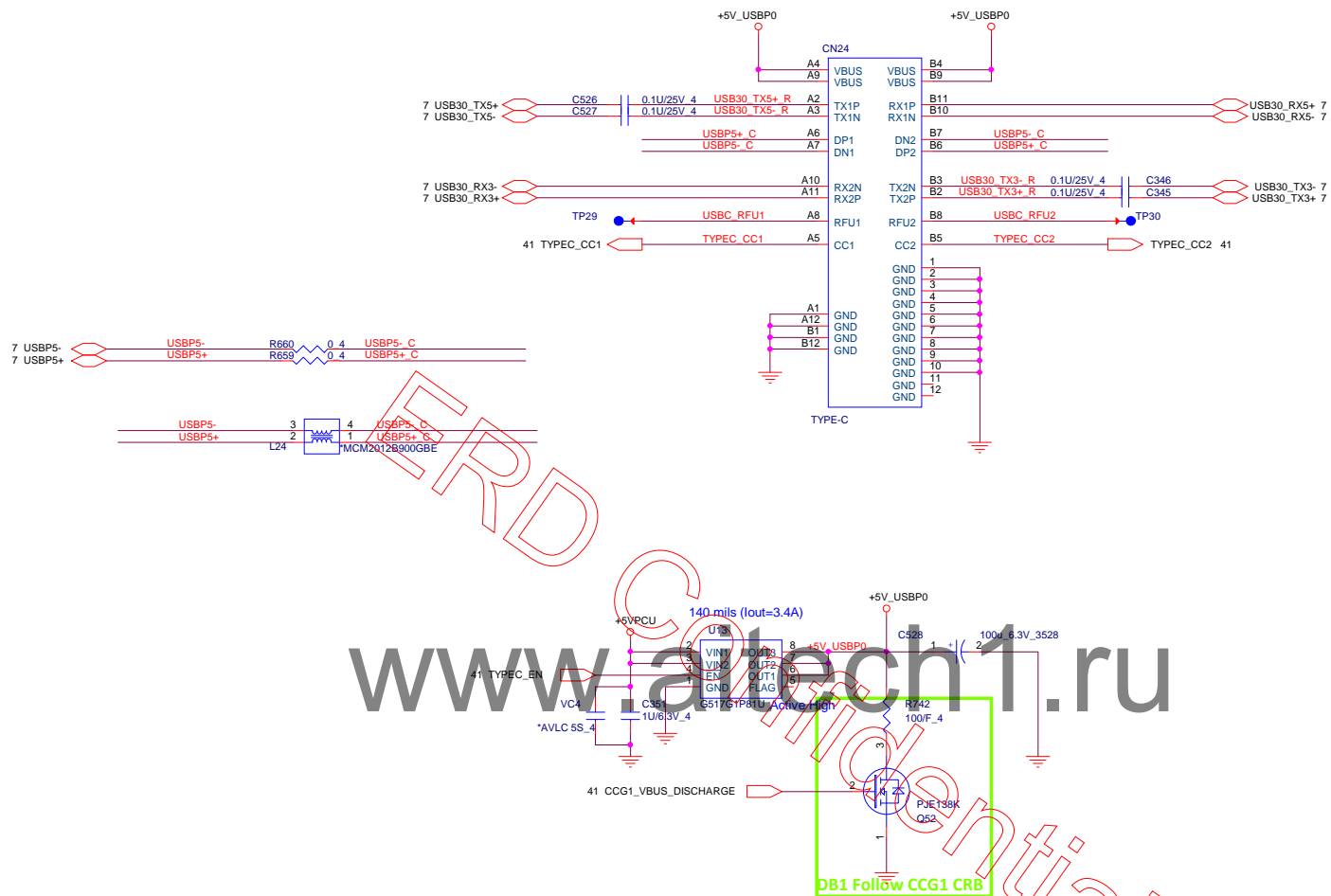
2,3,4,5,7,8,9,10,15,19,20,21,24,27,28,37,38,40,44,45,48,49,56,62,64

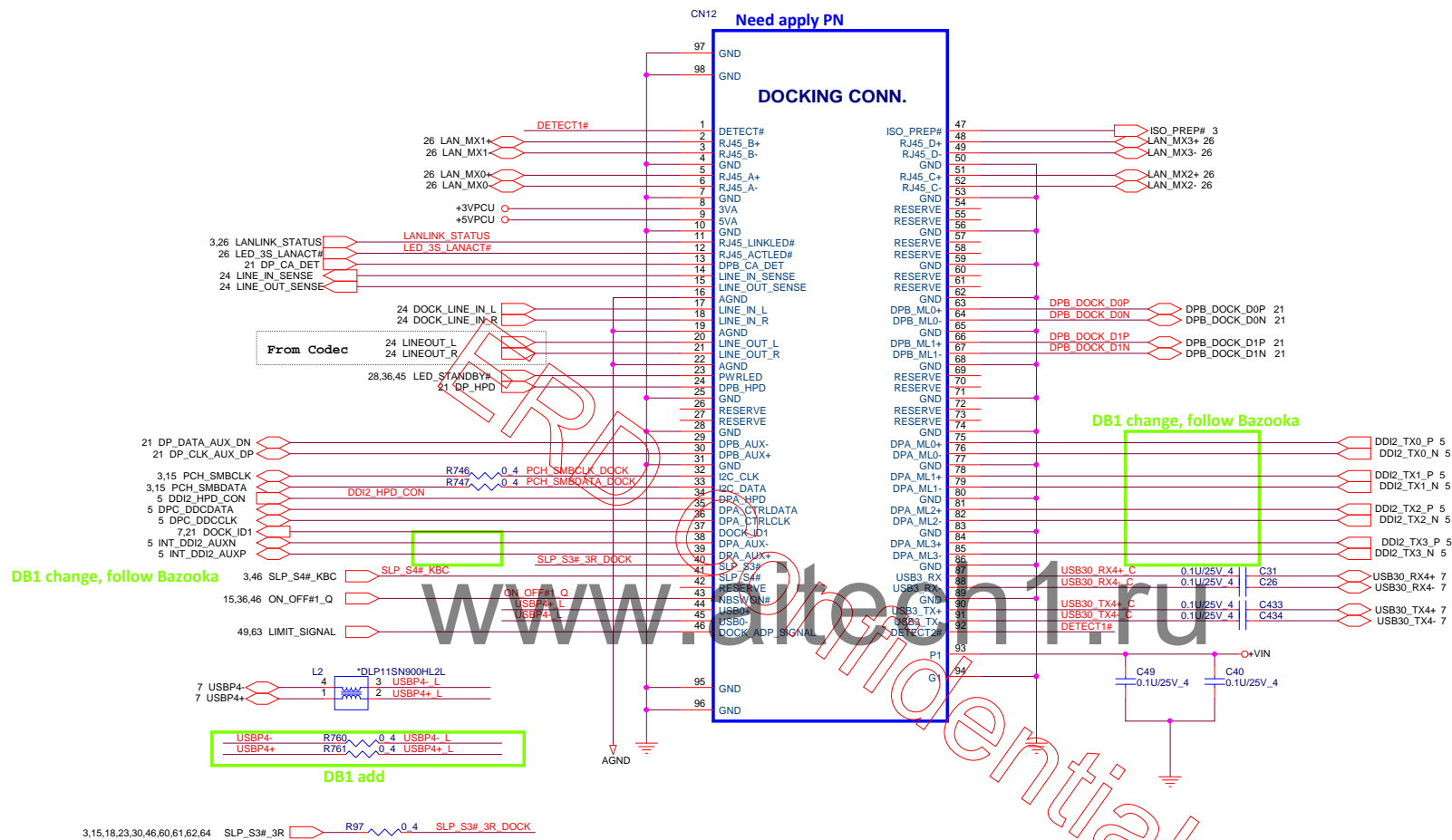


## NGFF-SSD

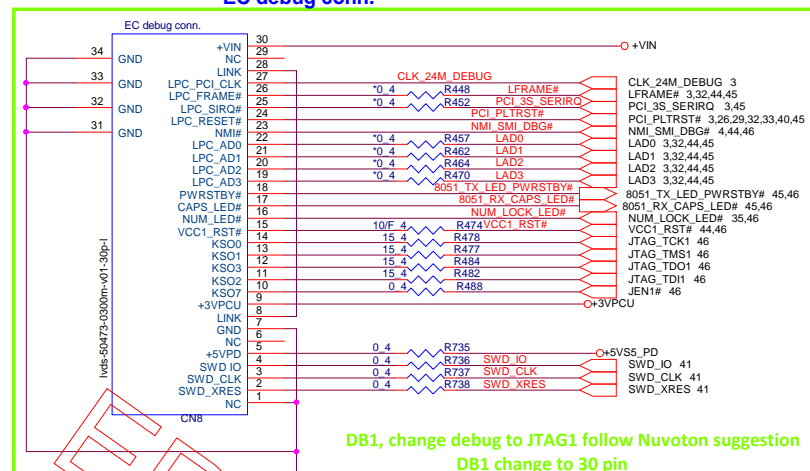




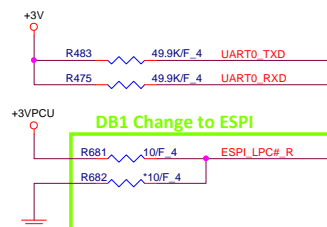




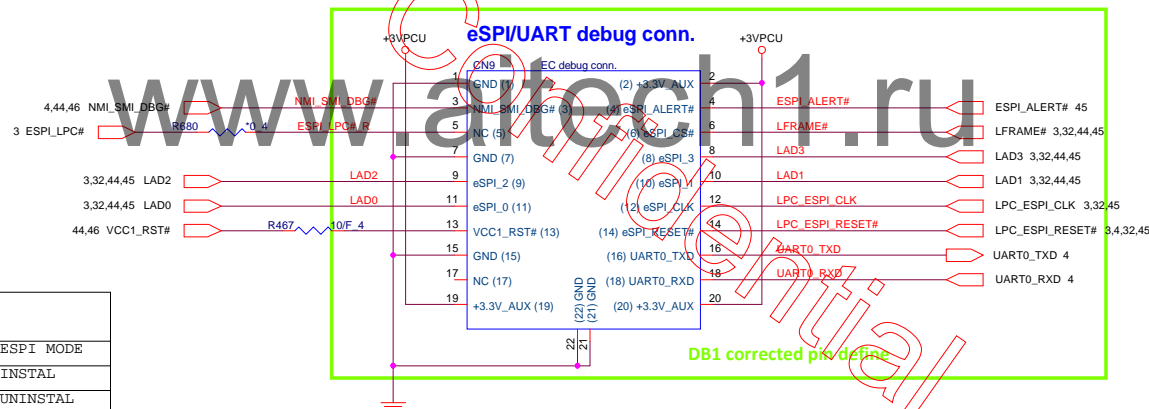
## EC debug conn.

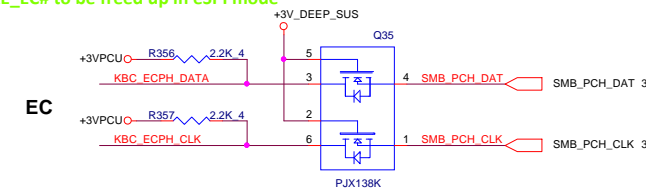


LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R448	INSTAL	UNINSTAL
R452	INSTAL	UNINSTAL
R457	INSTAL	UNINSTAL
R462	INSTAL	UNINSTAL
R464	INSTAL	UNINSTAL
R470	INSTAL	UNINSTAL

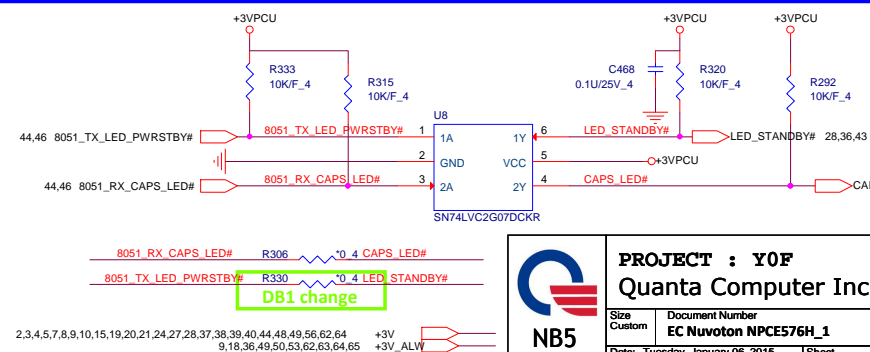
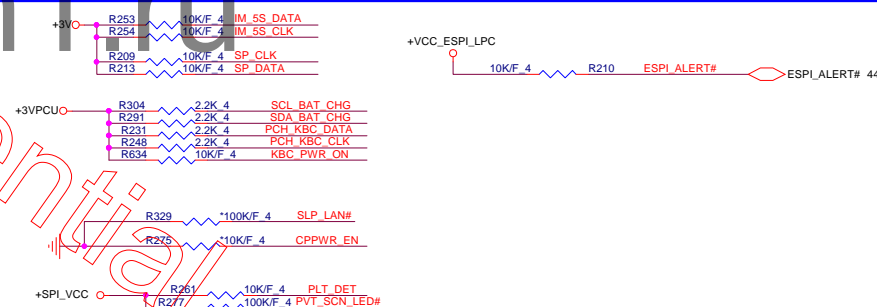


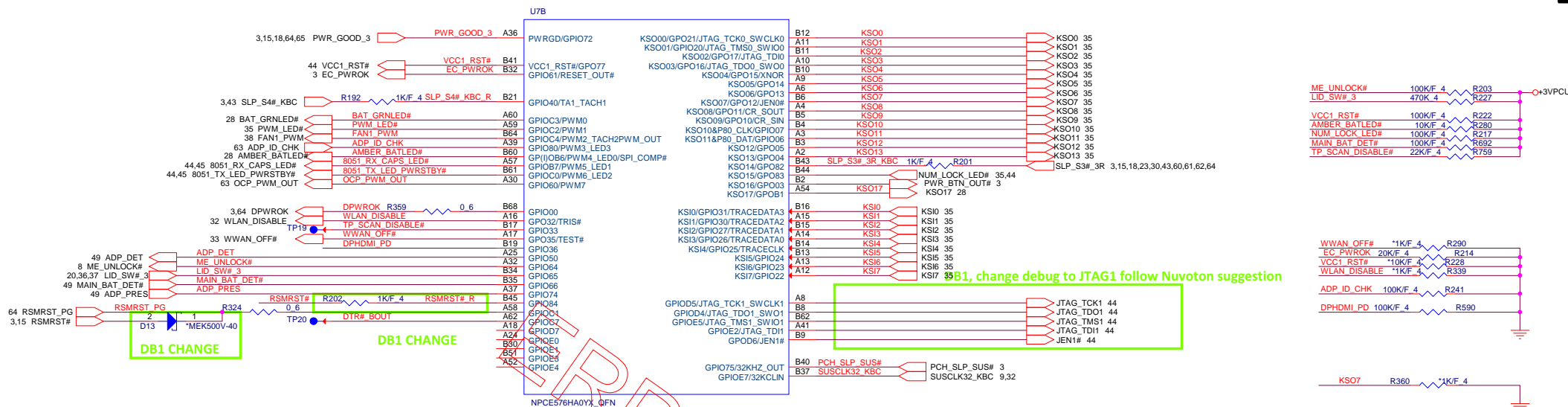
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R681	UNINSTAL	INSTAL
R682	INSTAL	UNINSTAL



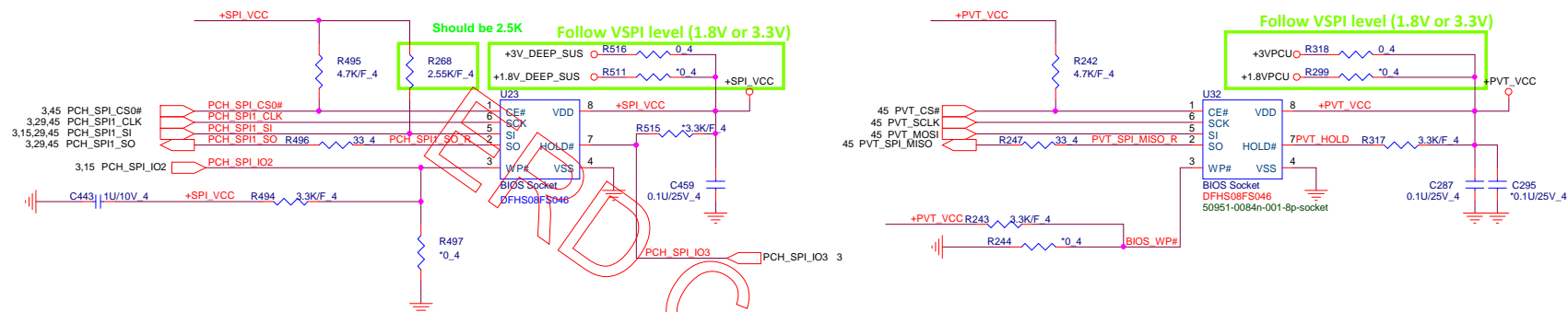


	Install	Un-Install
eSPI Mode	R218	R200
LPC Mode	R200	R218



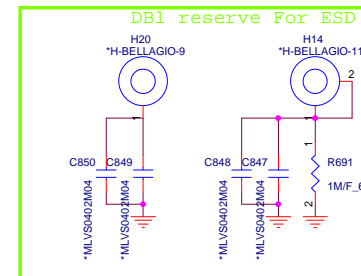
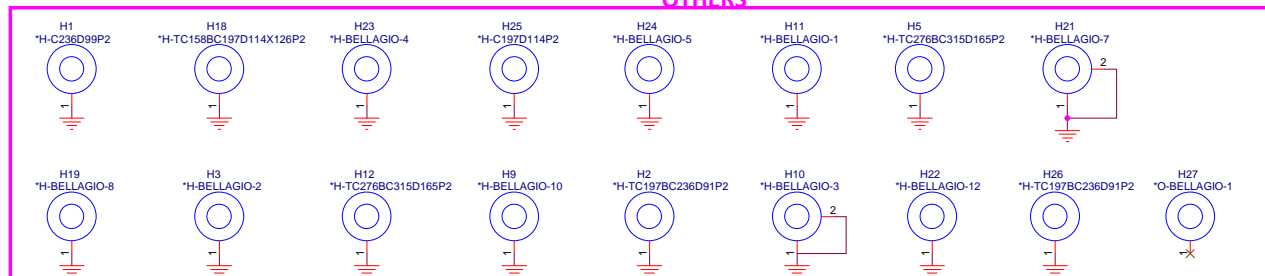




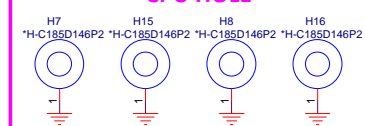


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## OTHERS



## CPU HOLE



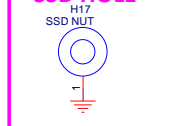
## WLAN HOLE



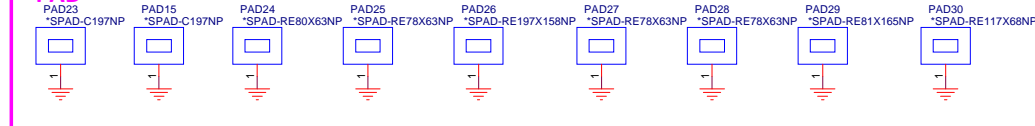
## WWAN HOLE



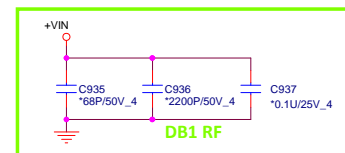
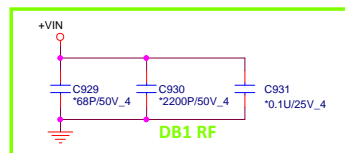
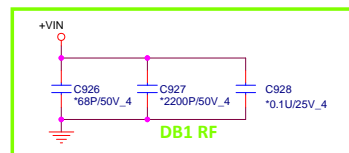
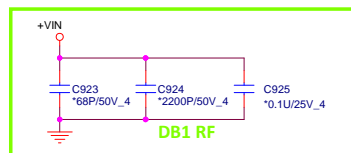
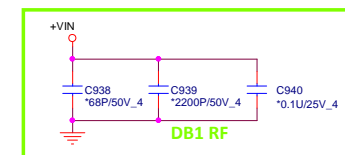
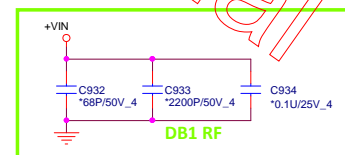
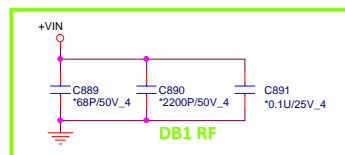
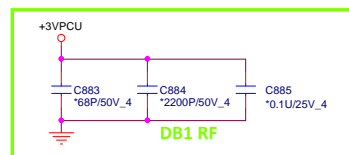
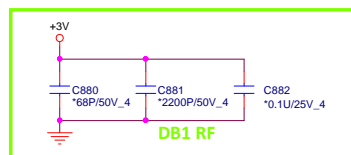
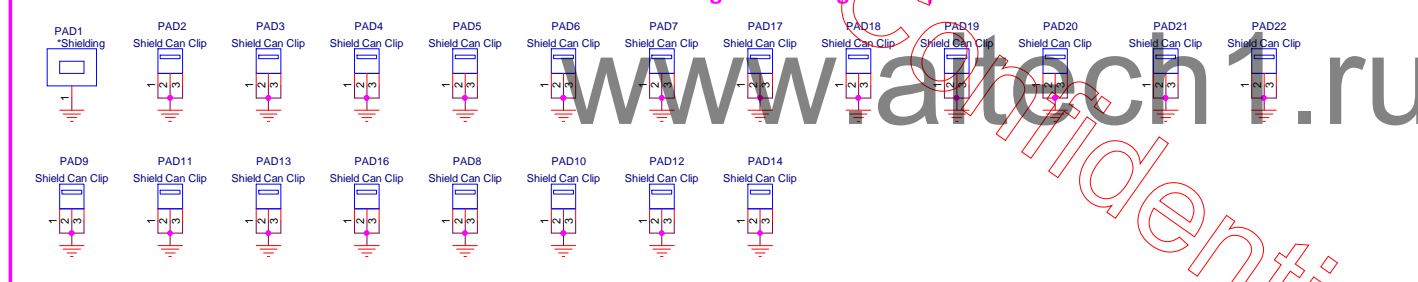
## SSD HOLE



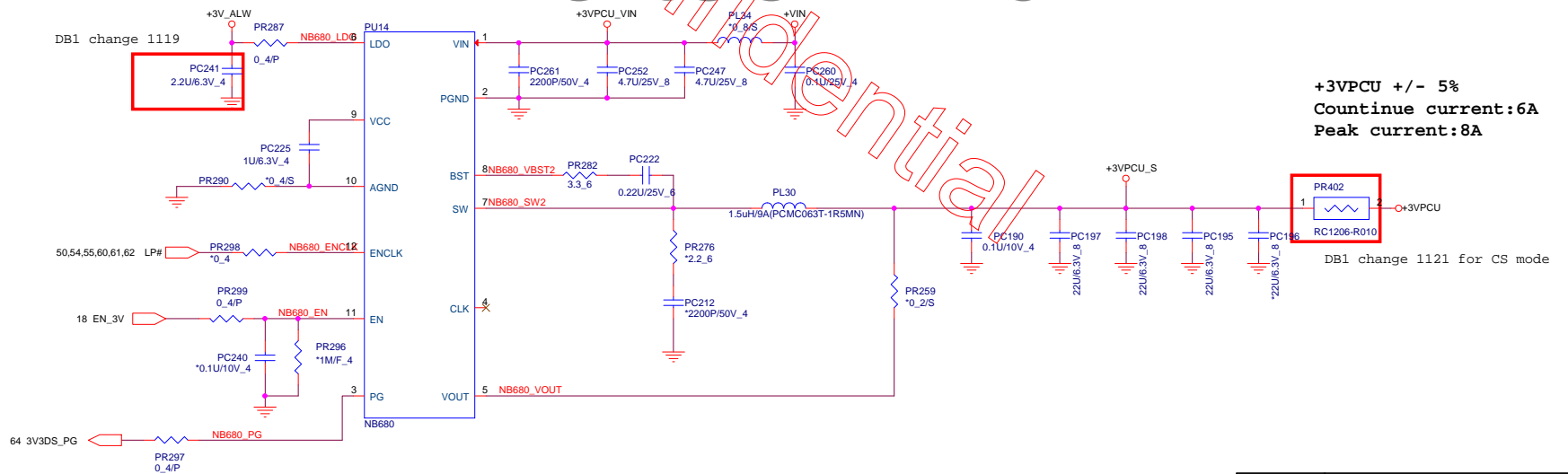
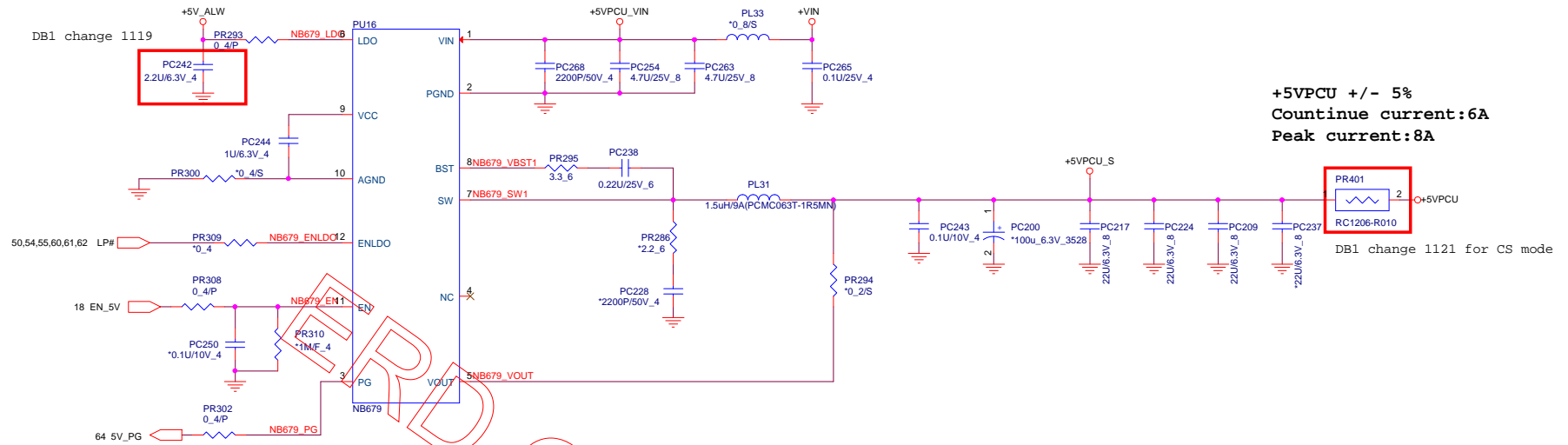
## PAD

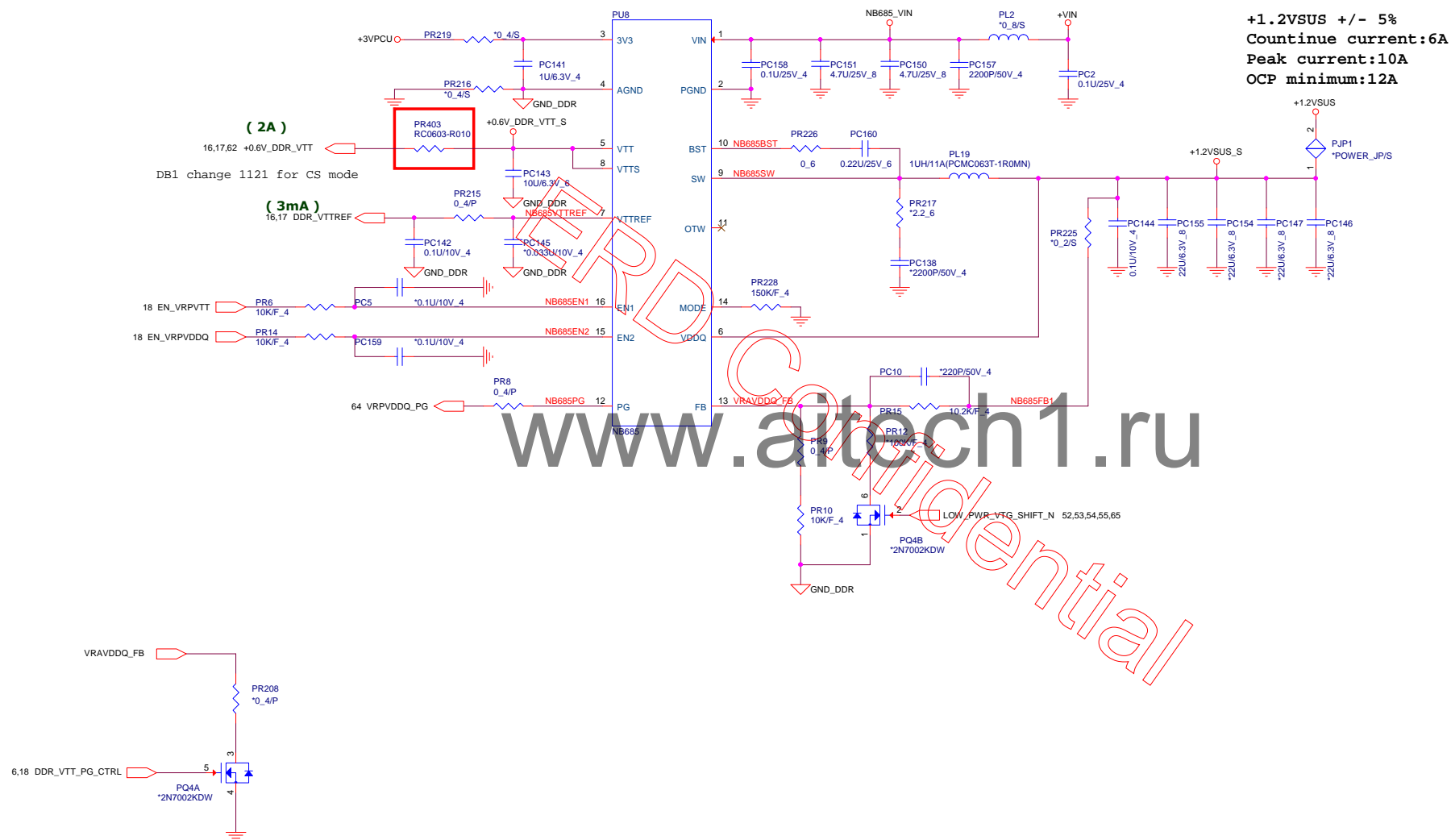


## Shielding &amp; Shielding Can Clip









20,43,44,48,49,50,51,53,54,55,57,58,59,60,61,66 +VIN  
 9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
 9,10,15,62,65 +1.0V\_DEEP\_SUS  
 +3VPCU  
 21 +1.5V

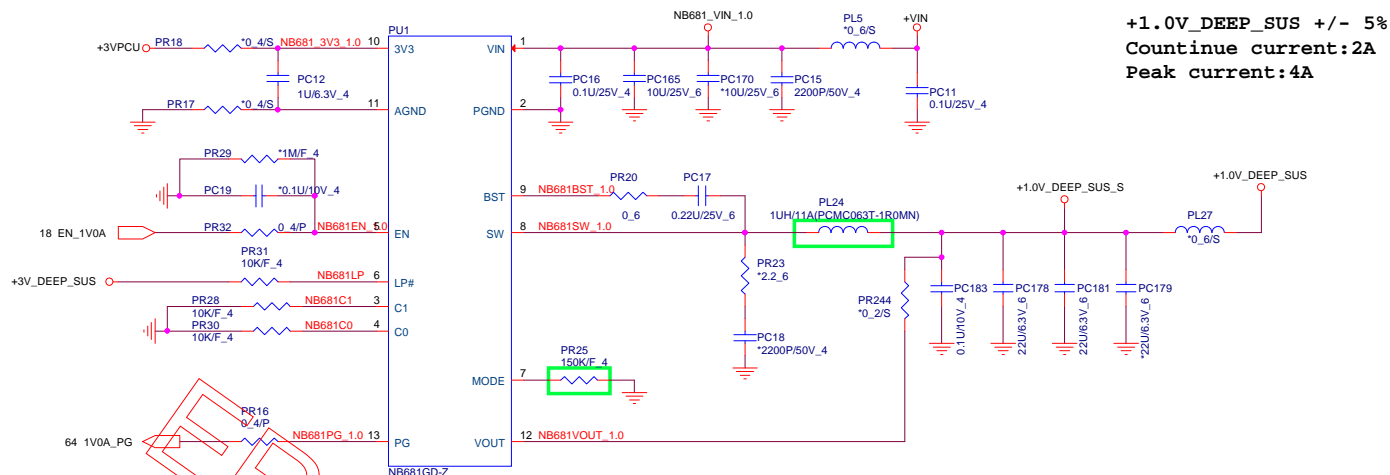
## other

LP#	C1	C0	Vout
0	X	X	0
1	0	0	1.0
1	0	1	1.075
1	1	0	1.15
1	1	1	1.2

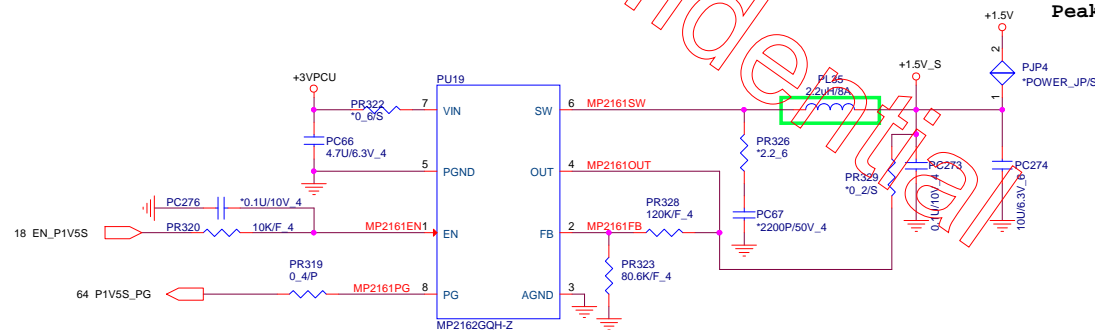
## MODE

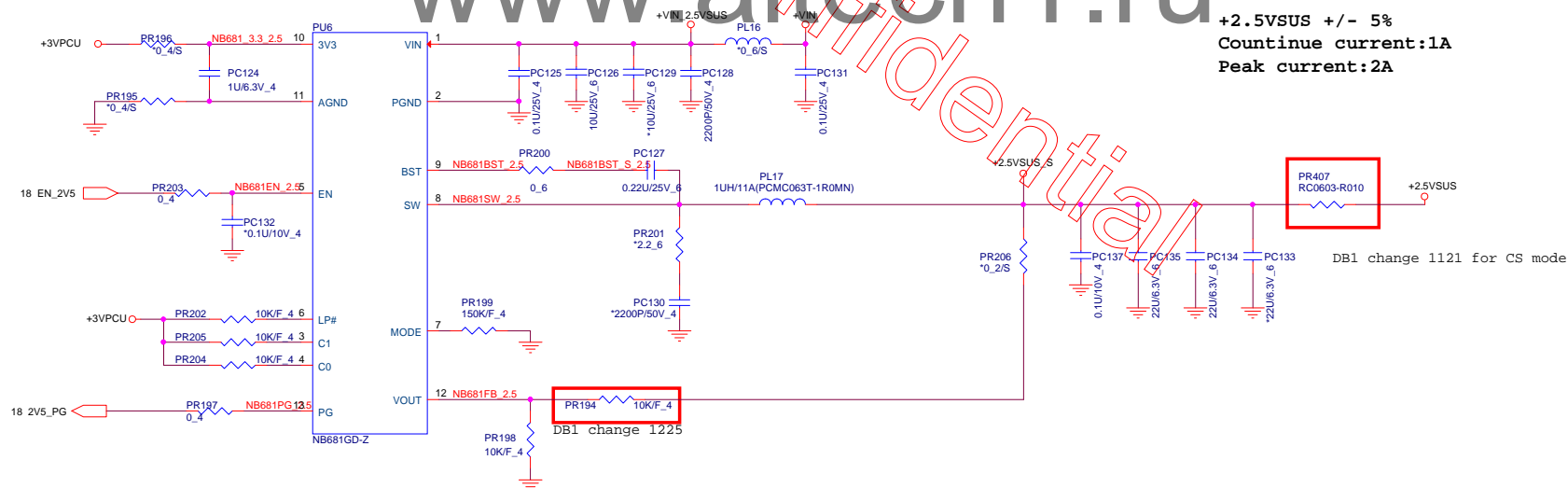
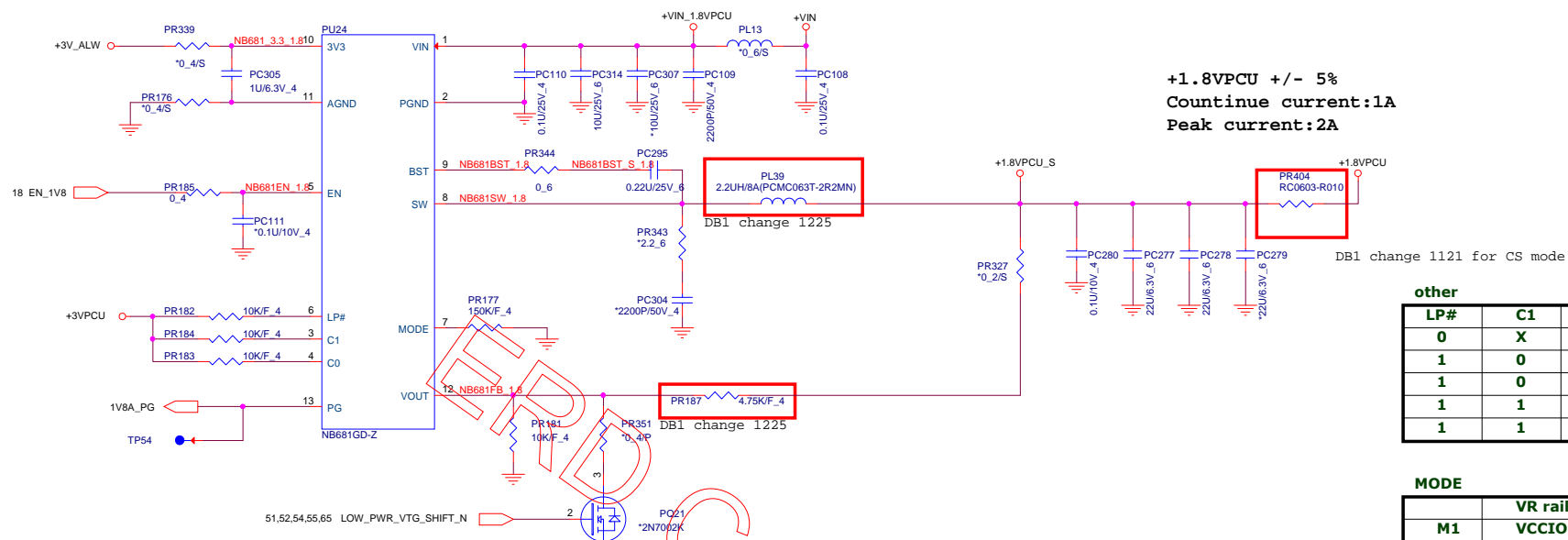
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

54,65 LOW\_PWR\_VTG\_SHIFT PR26 0.4P NB681C0  
 51,53,54,55,65 LOW\_PWR\_VTG\_SHIFT\_N PR27 0.4P NB681C1

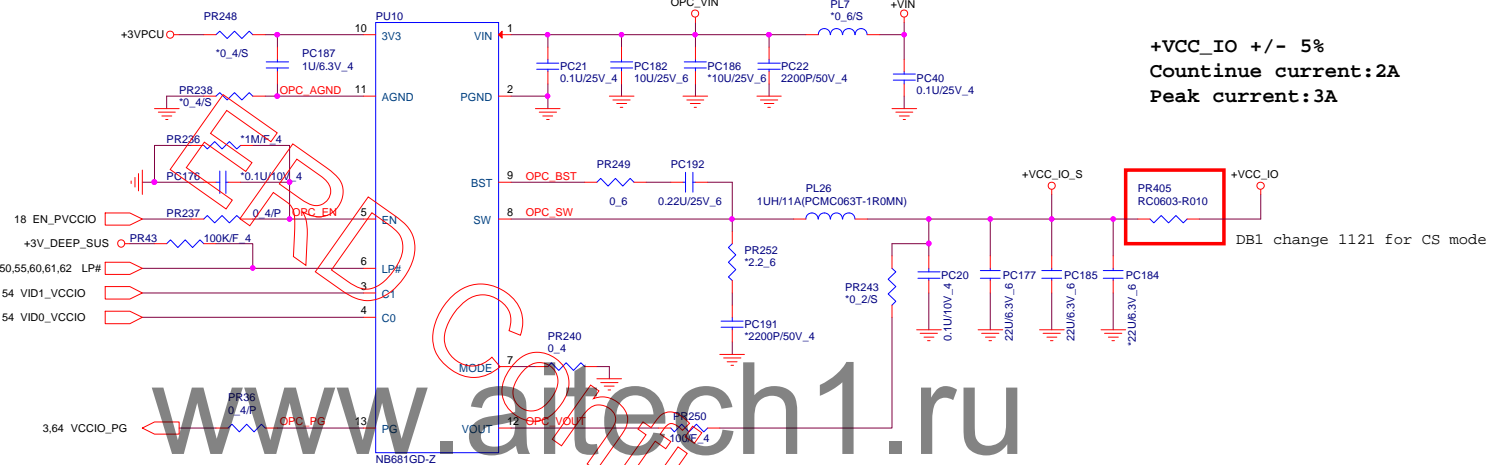
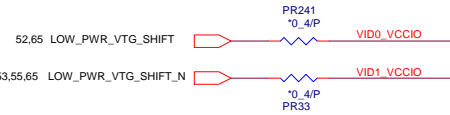
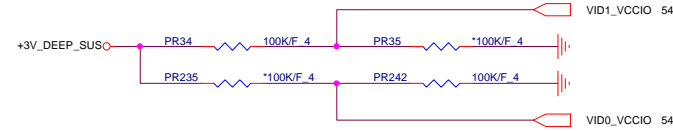


+1.5V +/- 5%  
 Countinue current:1A  
 Peak current:2A





20,43,44,48,49,50,51,52,53,55,57,58,59,60,61,66 +VIN  
9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
5,13,15 +VCC\_IO



**+VCC\_IO +/- 5%**  
**Countinue current:2A**  
**Peak current:3A**

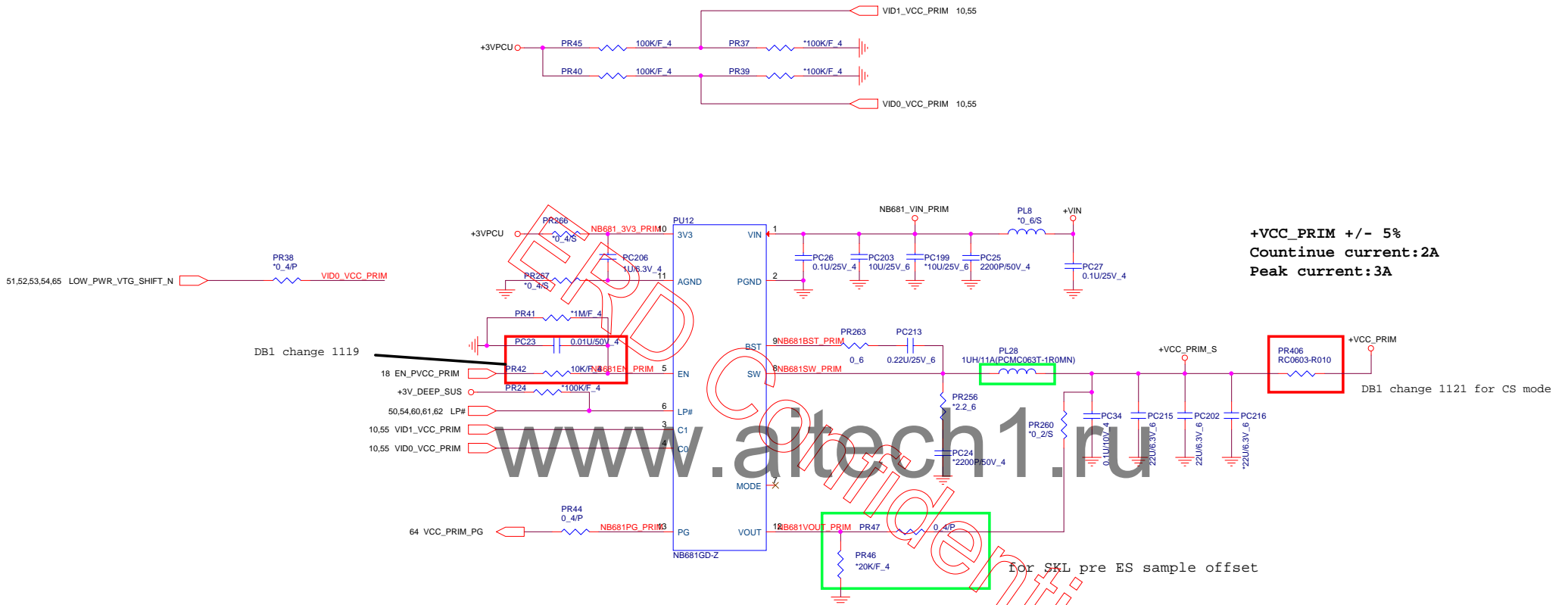
#### VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

#### MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K





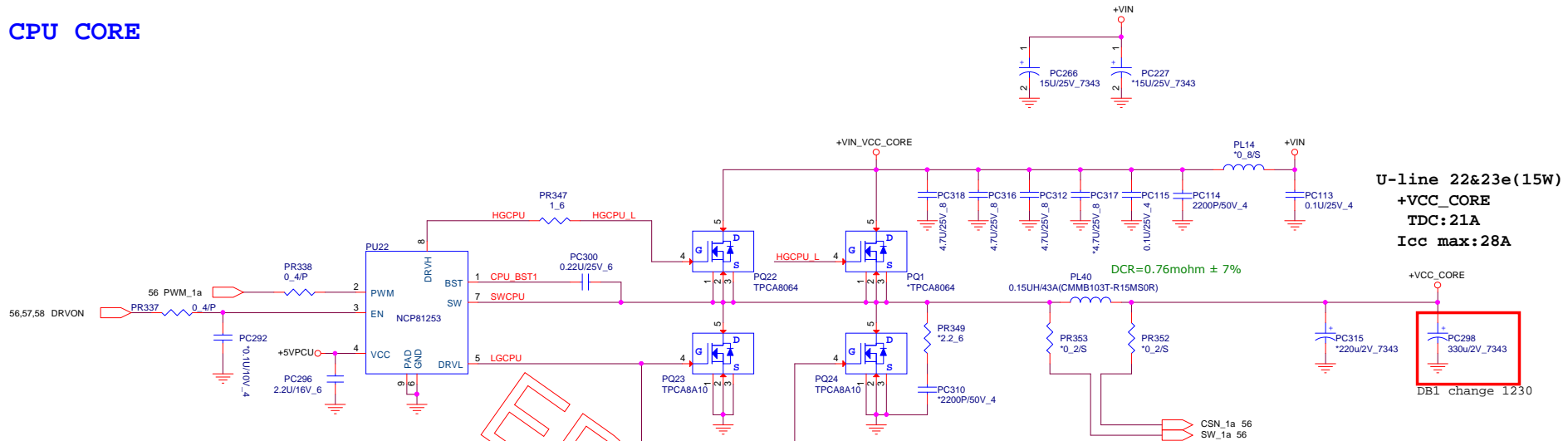
VCC\_PRIM

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPPIO	100K
M4	other	150K



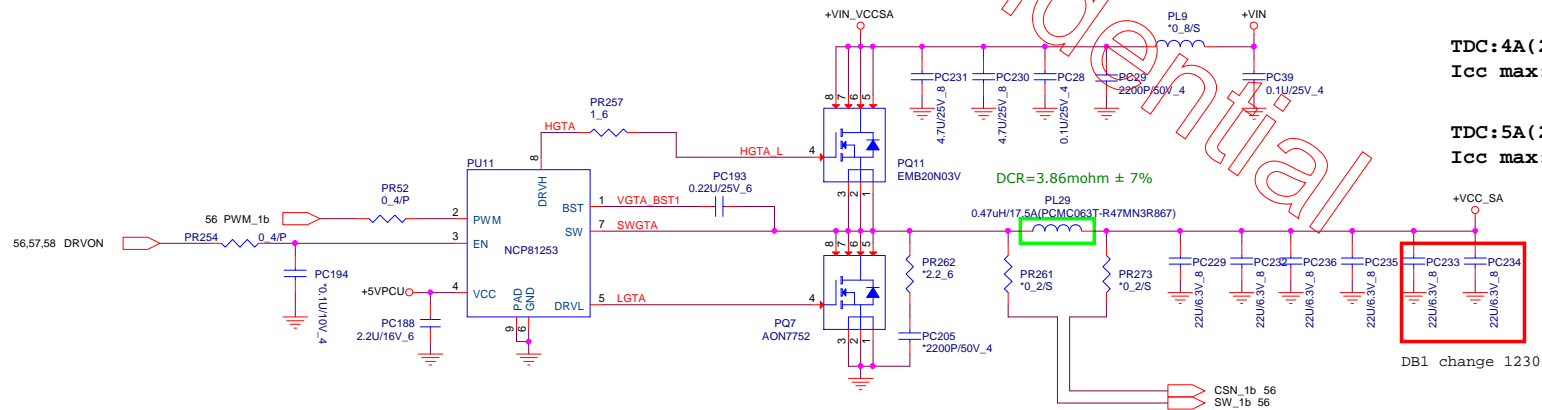


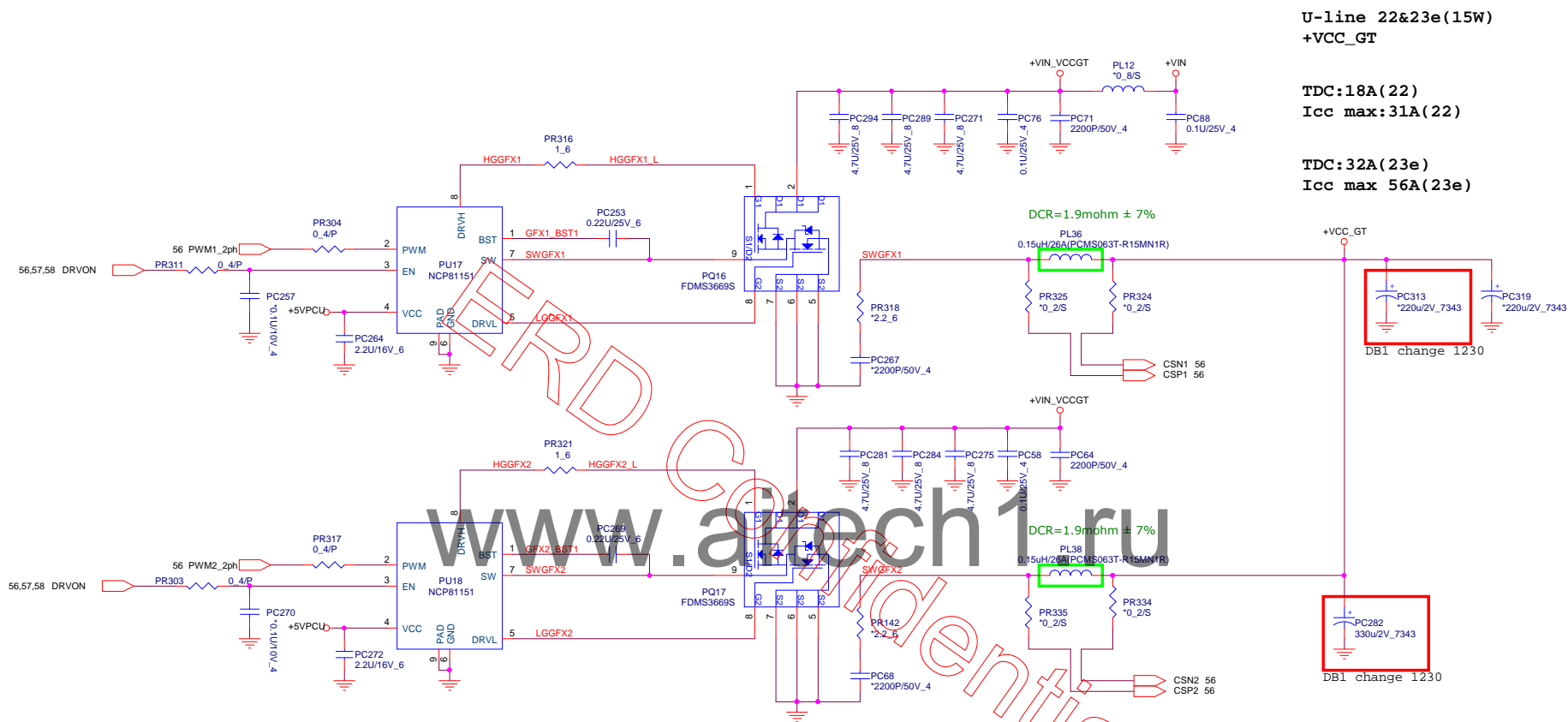
## VCCSA

U-line 22&23e(15W)  
+VCC\_SA

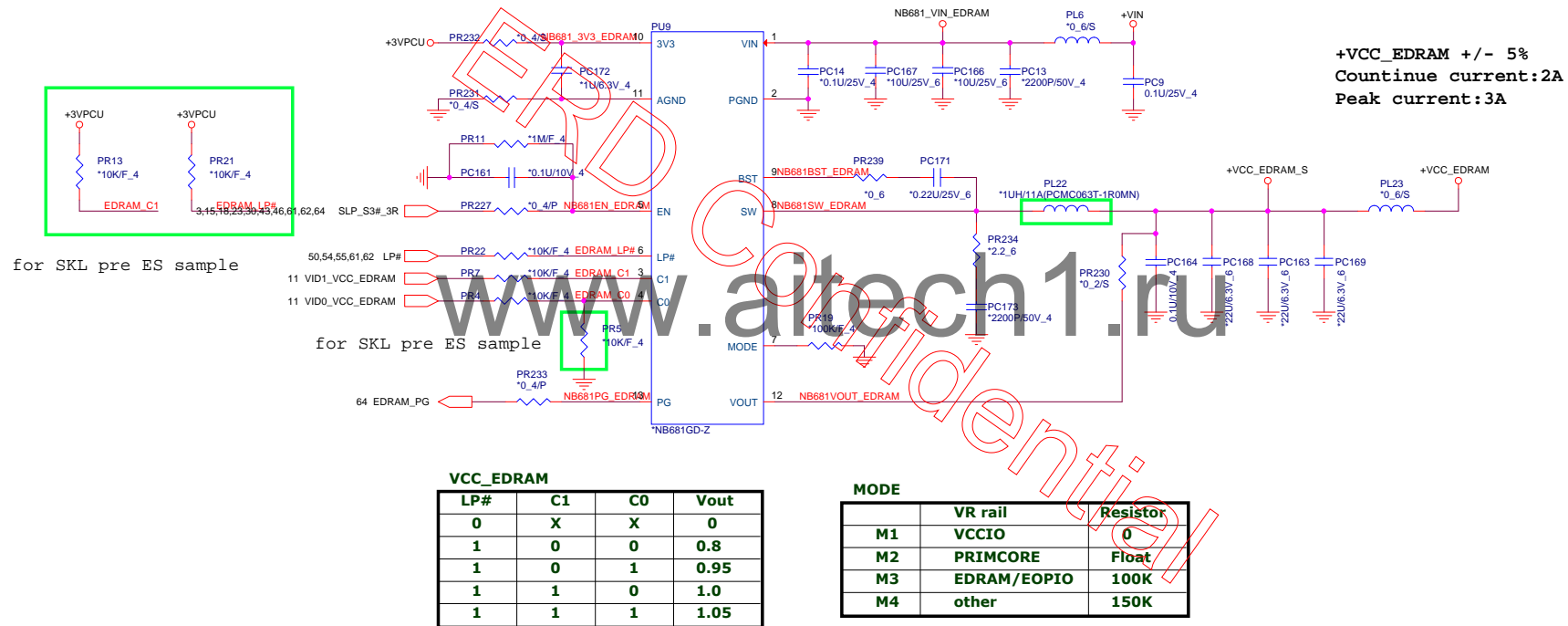
TDC: 4A(22)  
Icc max: 5A(22)

TDC: 5A(23e)  
Icc max: 5A(23e)

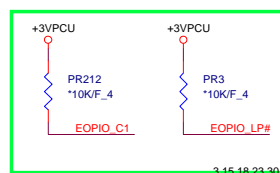




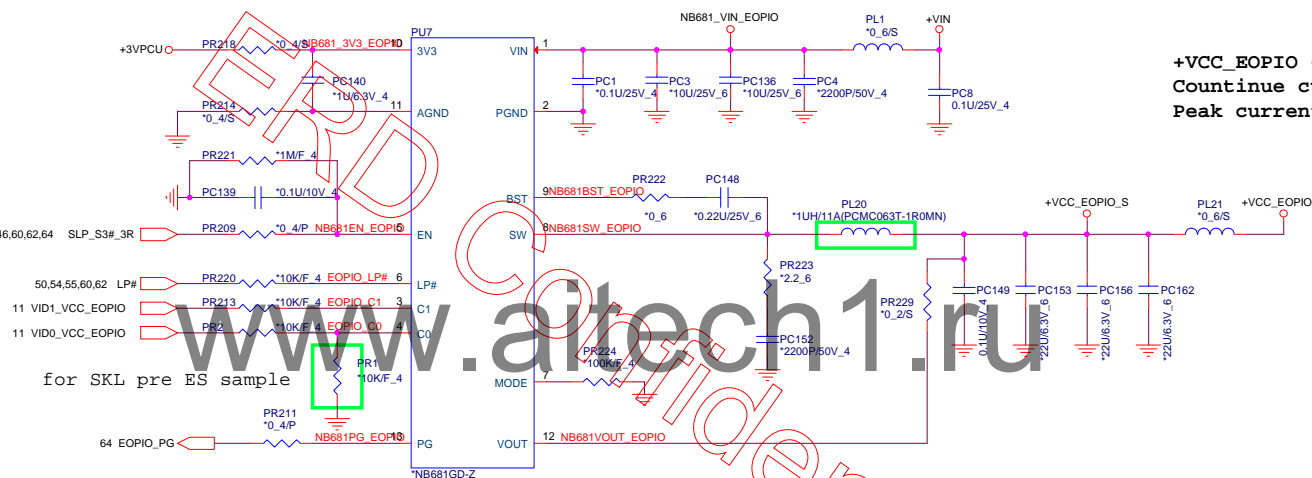




20,43,44,48,49,50,51,52,53,54,55,57,58,59,60,66 +VIN  
9,18,36,49,50,53,62,63,64,65 +3V\_ALW  
11 +VCC\_EOPIO



for SKL pre ES sample



+VCC\_EOPIO +/- 5%  
Countinue current:2A  
Peak current:3A

for SKL pre ES sample

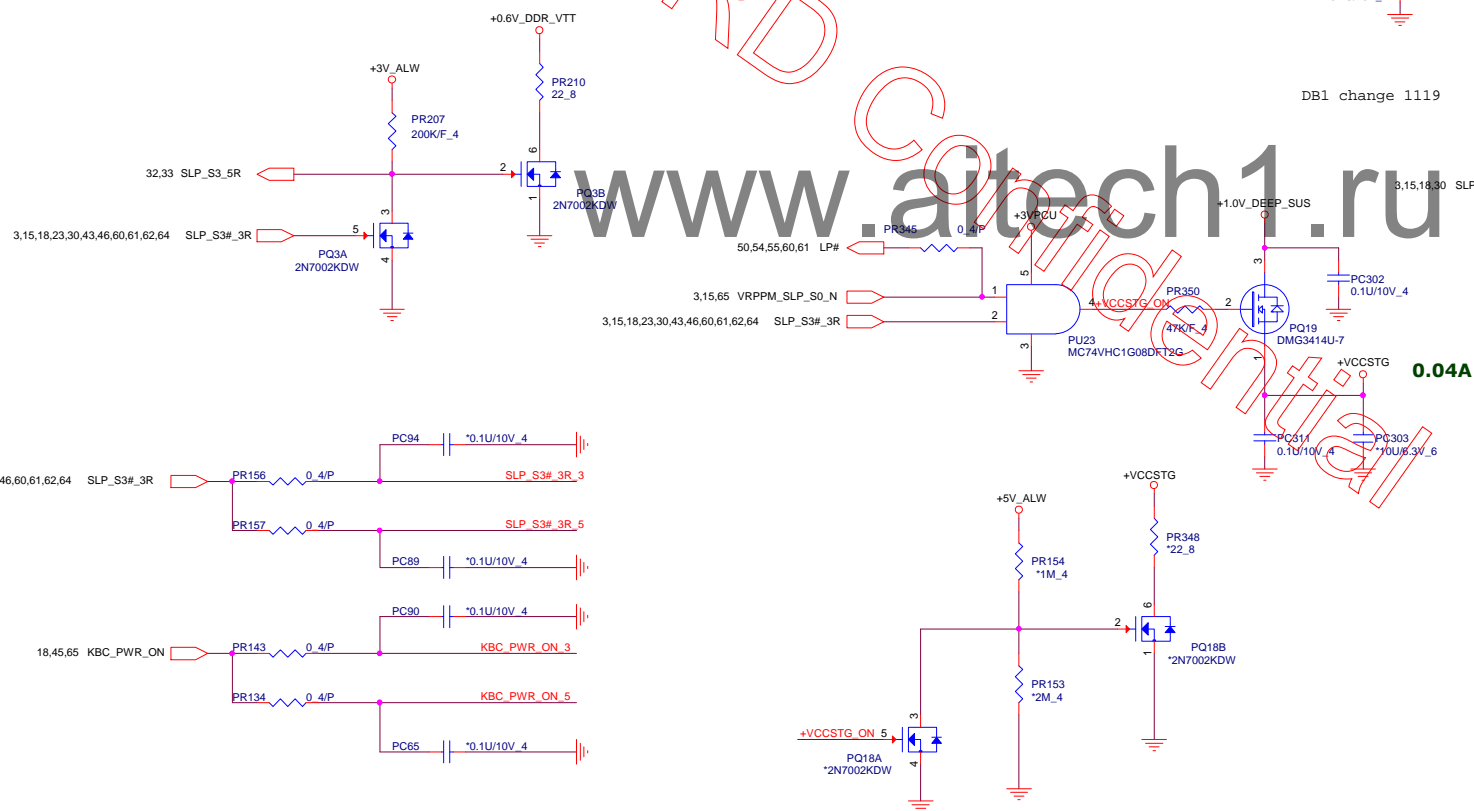
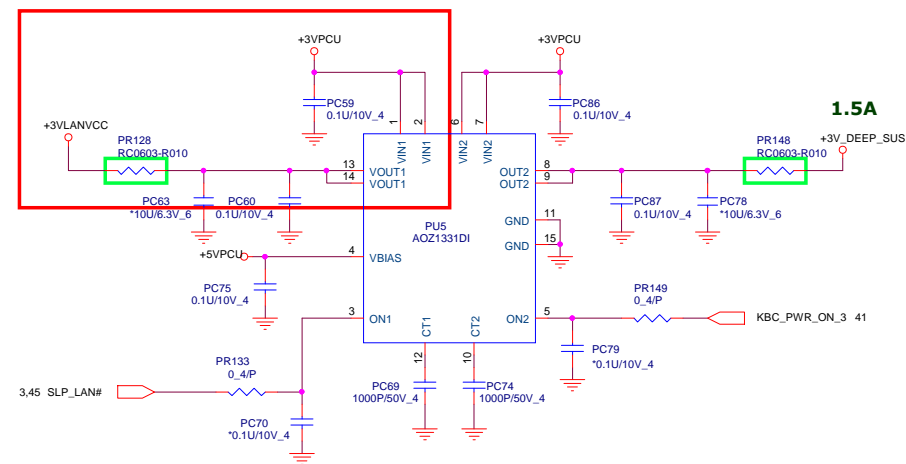
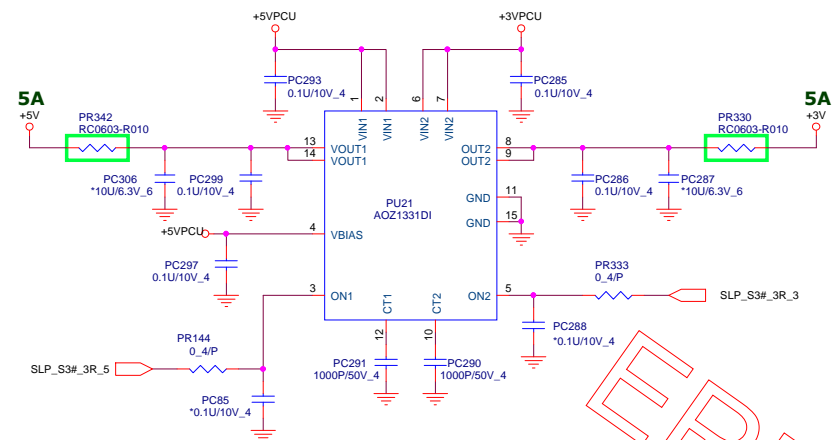
#### VCC\_EOPIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

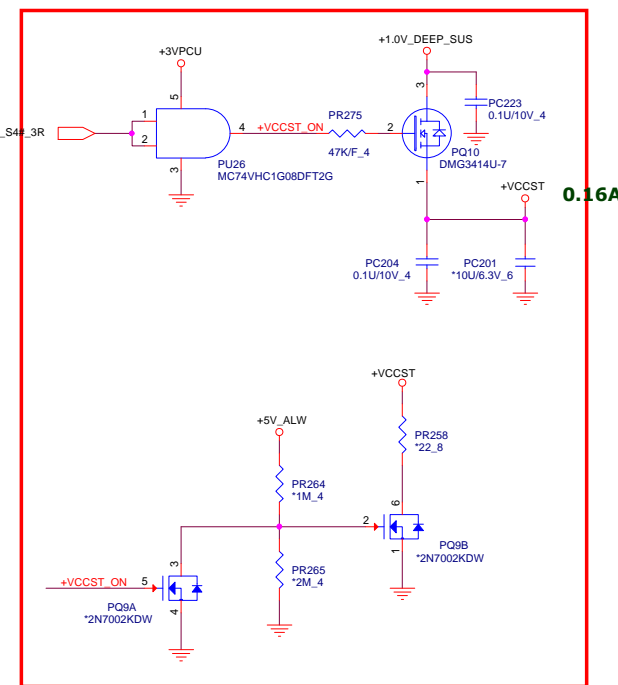
#### MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

DB1 change 1119



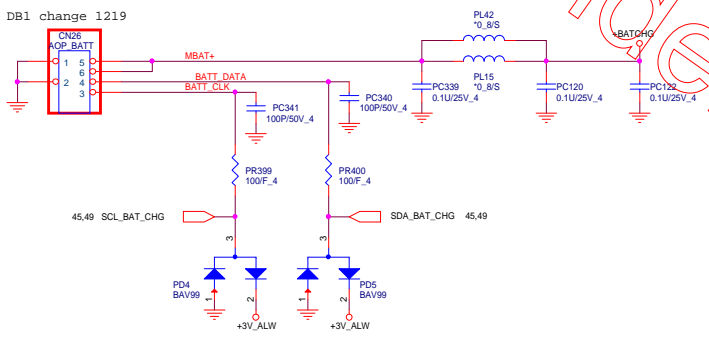
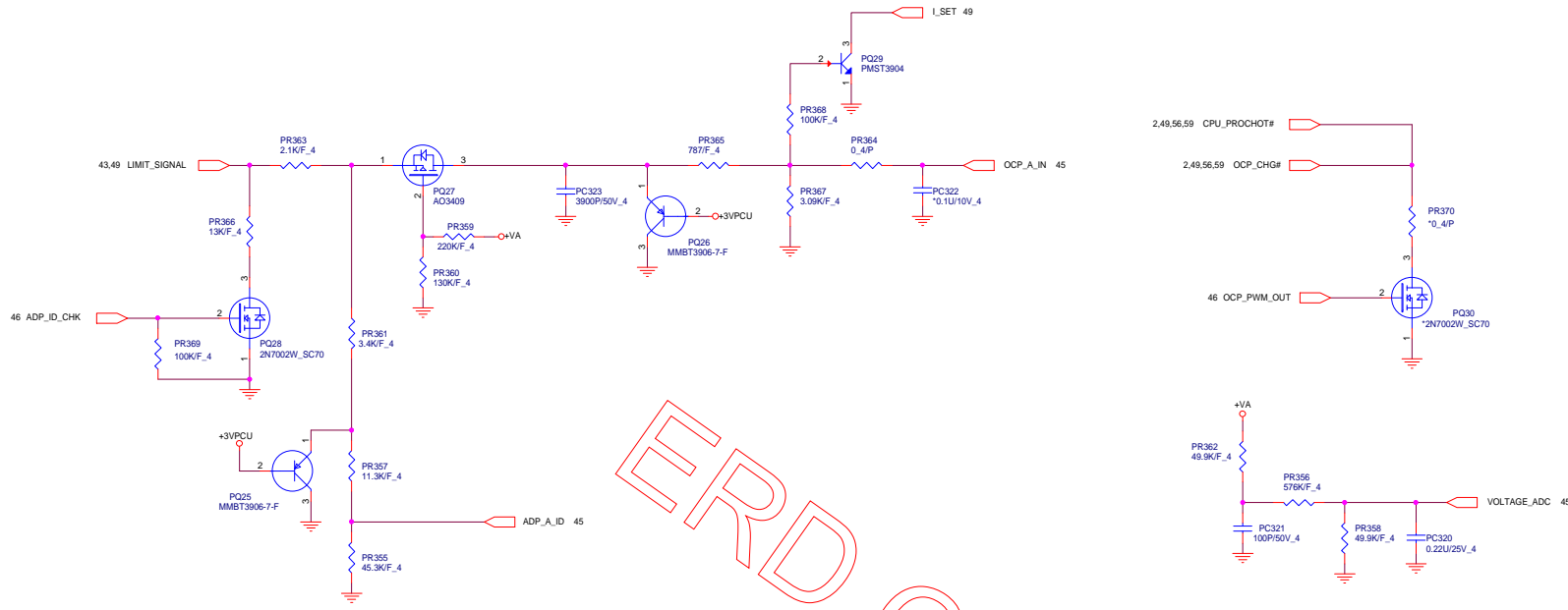
DB1 change 1119

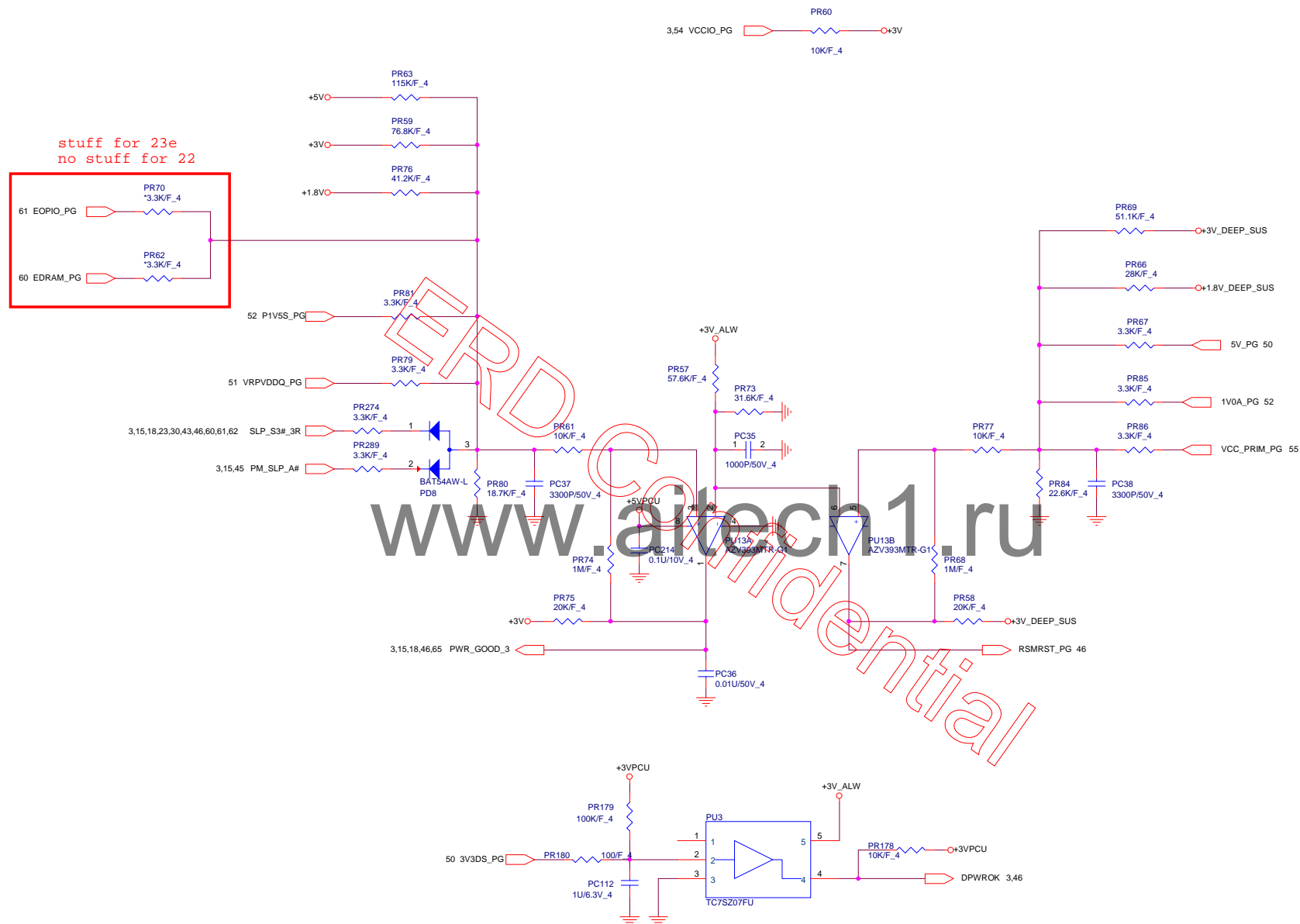


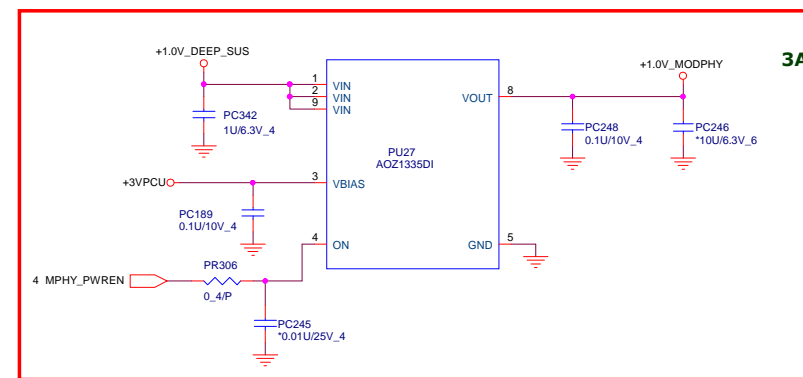
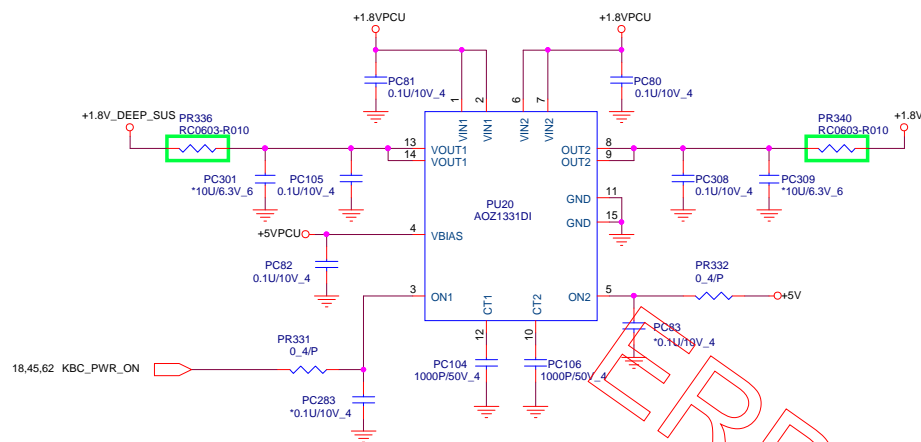
**PROJECT : Y0F**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Load switch (AOZ1331DI)	1A
Date: Tuesday, January 06, 2015	Sheet 62 of 67	

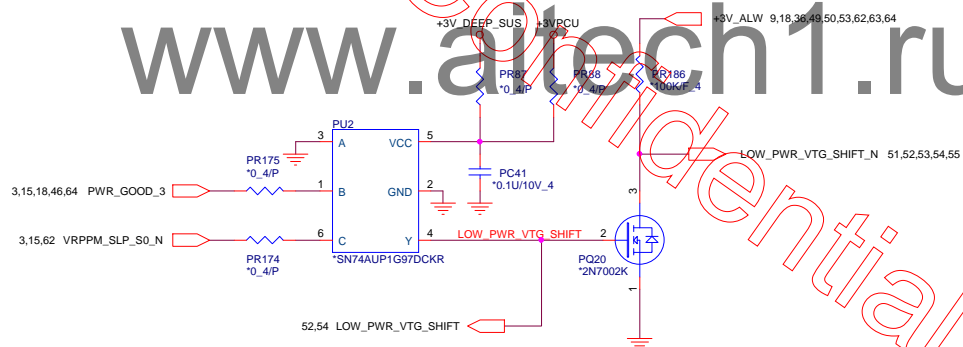






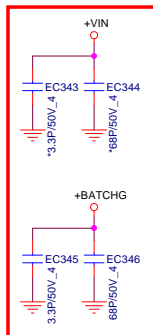


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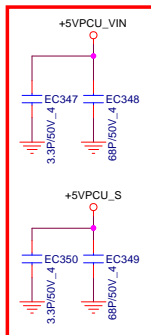


**Charger**

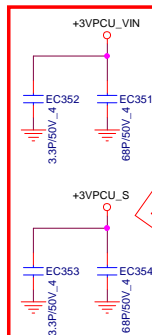
DB1 change 1222

**+5VPCU**

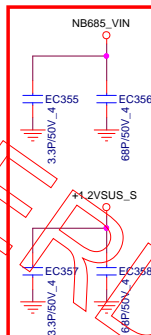
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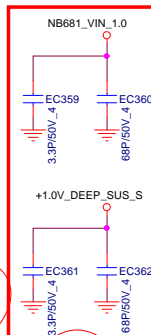
DB1 change 1222

**+1.2VSUS**

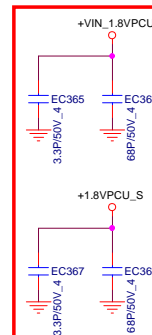
DB1 change 1222

**+1.0V\_DEEP\_SUS**

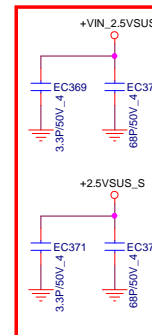
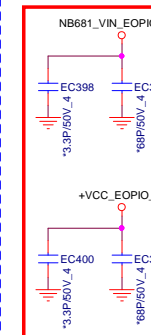
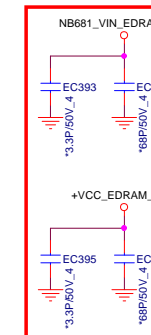
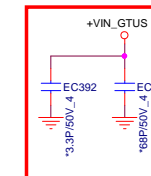
DB1 change 1222

**+1.8VPCU**

DB1 change 1222

**+2.5VSUS**

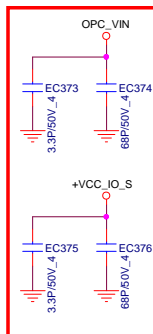
DB1 change 1222

stuff for 23e  
no stuff for 22**+VCC\_EOPIO****+VCC\_EDRAM****+VCC\_GTX**

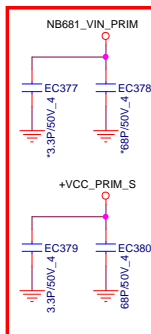
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**+VCC\_IO**

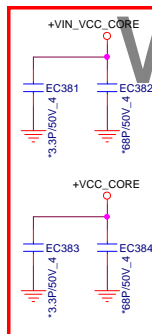
DB1 change 1222

**+VCC\_PRIM**

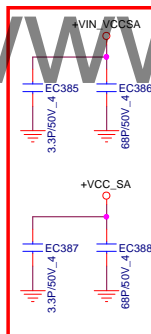
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**+VCC\_CORE**

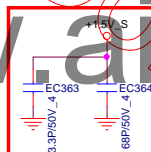
DB1 change 1222

**+VCC\_SA**

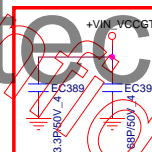
DB1 change 1222

**+1.5V**

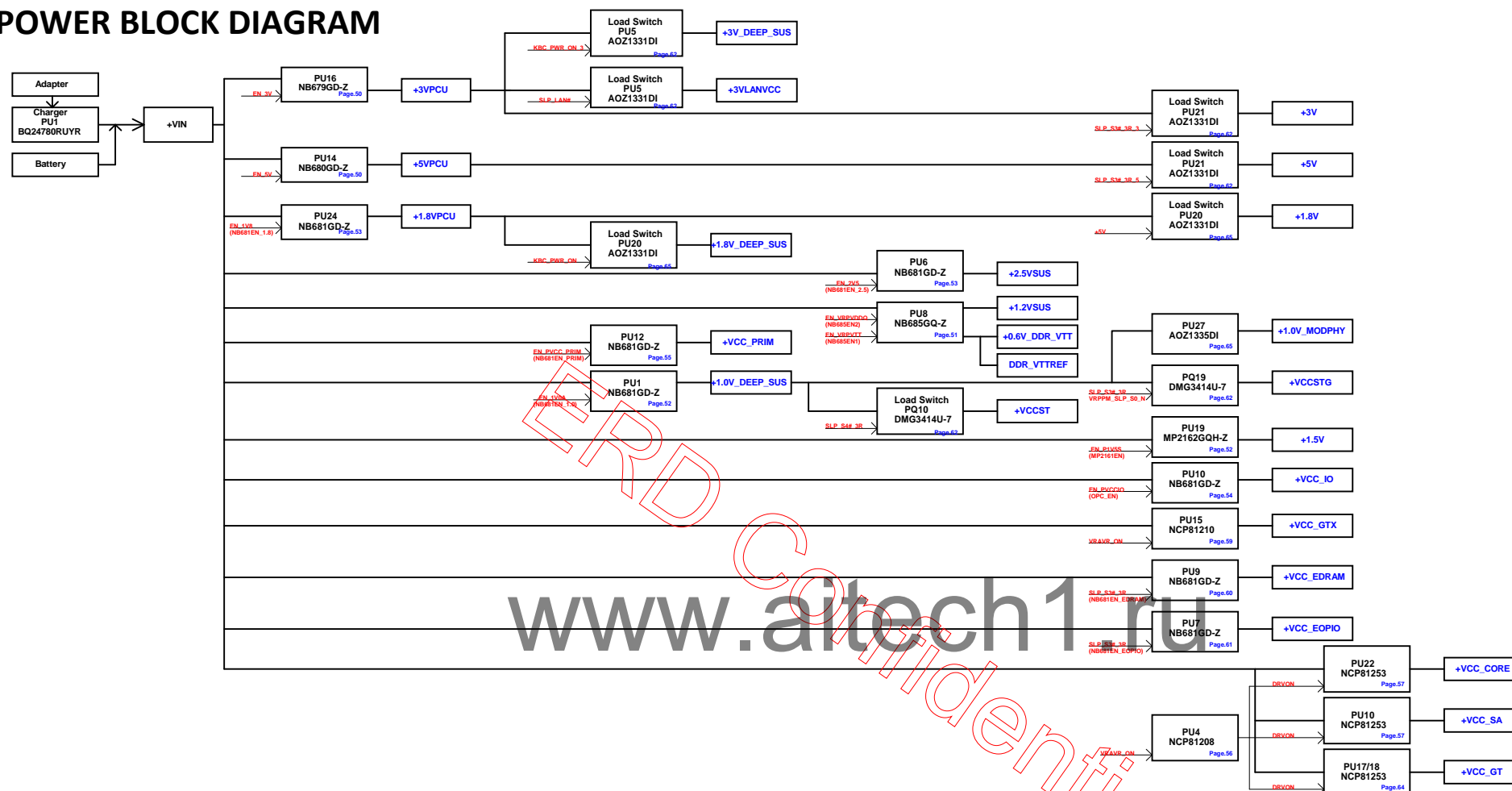
DB1 change 1222

**+VCC\_GT**

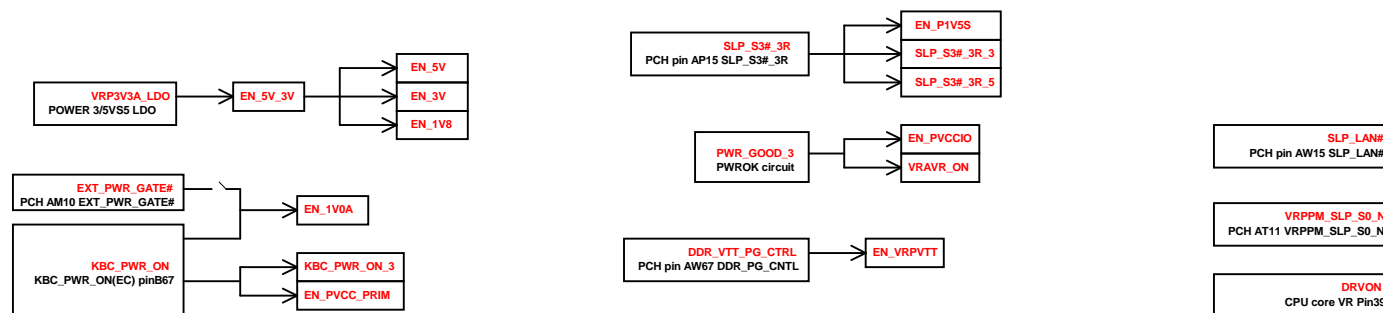
DB1 change 1222

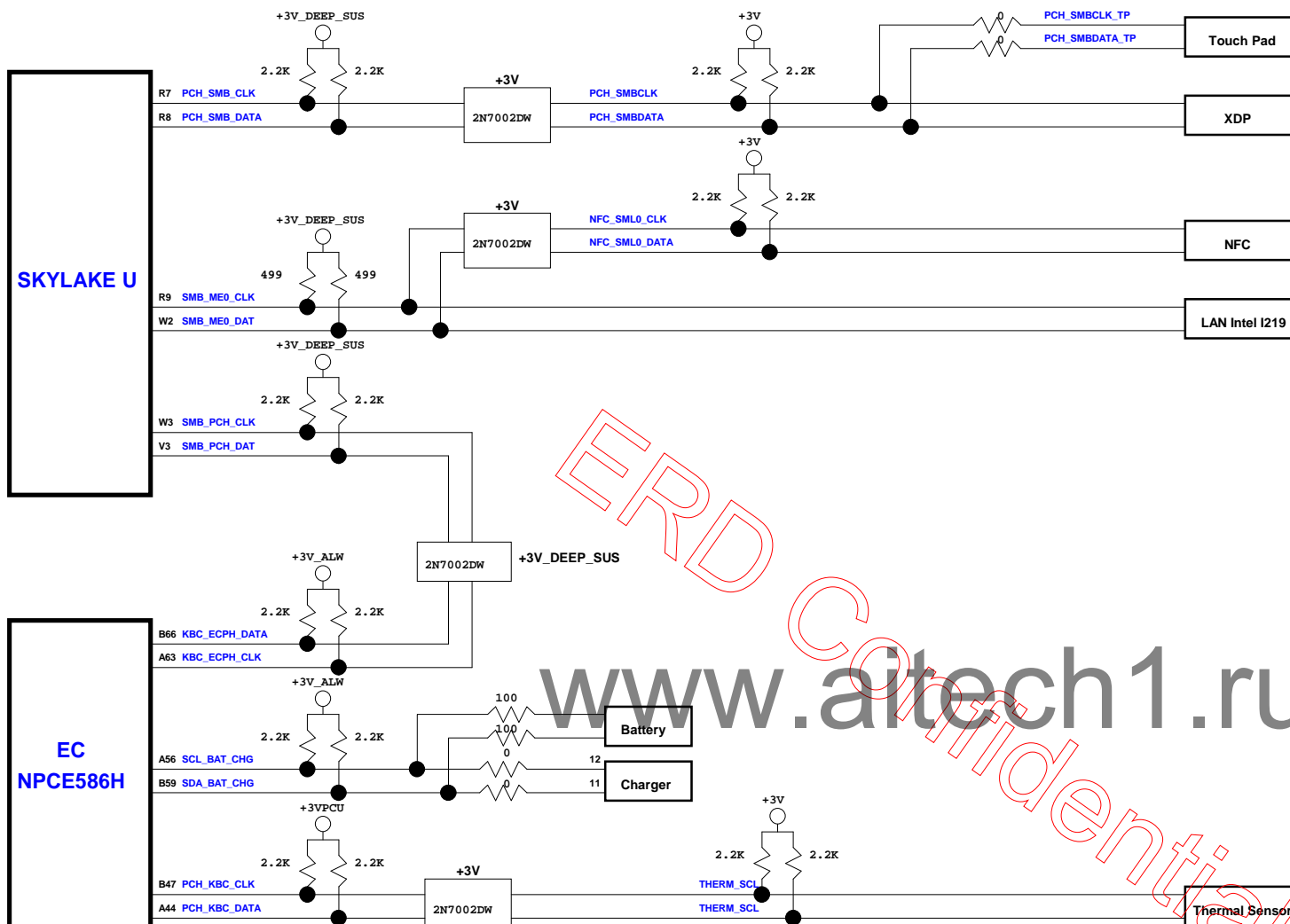


## POWER BLOCK DIAGRAM



## POWER ENABLE PIN





Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	USB3.0 Dock
PCIE1 / USB3 #5	USB3.1 (Type-C)
PCIE2 / USB3 #6	NC
PCIE3	NC
PCIE4	NC
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	NC
PCIE8 / SATA #1	NC
PCIE9	SSD (SATA)
PCIE10	SSD (SATA)
PCIE11 / SATA #1*	SSD (SATA)
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Dock)
USB2 #5	USB2.0(Type-C)
USB2 #6	NC
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	SmartCard